MICROCHIP **PIC18F2220/2320/4220/4320**

PIC18F2220/2320/4220/4320 Data Sheet Errata

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS39599**G**), the following clarifications and corrections should be noted. Any silicon issues related to the PIC18F2220/2320/4220/4320 will be reported in a separate silicon errata. Please check the Microchip web site for any existing issues.

1. Module: Power-Managed Modes

- In the third paragraph of **Section 3.3.3** “**RC_IDLE Mode**” on page 35, the IOFS bit set time is changed. The modified value is indicated in bold text:

  If the IRCF bits are set to a non-zero value (thus enabling the INTOSC output), the IOFS bit becomes set after the INTOSC output becomes stable, in about **128 μs**.

- In the sixth paragraph of **Section 3.4.3** “**RC_RUN Mode**” on page 37, the INTOSC clock source stabilizing time has changed. The modified value is indicated in bold text in the following excerpt of the section:

  If the IRCF bits are changed from all clear (thus enabling the INTOSC output), the IOFS bit becomes set after the INTOSC output becomes stable. Clocks to the system continue while the INTOSC source stabilizes in approximately **128 μs**.

2. Module: Oscillator Configurations (INTRC)

- The first, third, fourth and fifth paragraphs of **Section 2.6.2** “**OSCTUNE Register**” on page 23 have been modified:
  - First paragraph:

    The internal oscillator block is calibrated at the factory to produce an INTOSC output frequency of approximately 8 MHz. (See parameters F14 **through** F19 in Table 26-8).
  - Third paragraph:

    The tuning sensitivity is constant throughout the tuning range. This sentence is deleted.
  - Fourth paragraph:

    OSCTUNE register does not affect the INTRC frequency. The modified value is indicated in bold text.

    When the OSCTUNE register is modified, the INTOSC frequency begins shifting to the new frequency. The INTOSC clock will stabilize at the new frequency within 100 μs. Code execution continues during this shift.
  - Fifth paragraph:

    Except for the first sentence (**There is no indication when the shift occurs**), the remaining content is deleted.

REGISTER 2-1: OSCTUNE: OSCILLATOR TUNING REGISTER values are modified.

In the description of bit 0, the second sentence is deleted, and the modified content is indicated in bold text in Register 2-1.

REGISTER 2-1: OSCTUNE: OSCILLATOR TUNING REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 Unimplemented: Read as ‘0’

bit 5-1 TUN<5:1>: Frequency Tuning bits – Adjusts the frequency of INTOSC. Can adjust INTRC, depending on TUNSEL (OSCTUN2<7>)

011111 = Maximum frequency
•
•
000001
000000 = Center frequency. Oscillator module is running at the calibrated frequency
111111
•
•
100000 = Minimum frequency

bit 0 **TUN<0>: This bit is a placeholder and has no effect on the INTOSC frequency.**

3. Module: OSCTUN2 REGISTER

The bullet points in the second paragraph of **Section 2.6.3** "**OSCTUN2 Register**" on page 24 are modified. The modified values indicate that the OSCTUNE register does not affect the INTRC frequency. The modified values are indicated in bold text in the following excerpt of the section:

- **If TUNSEL (OSCTUN2<7>) is clear – The INTOSC clock frequency can be adjusted by the TUN5:TUN1 bits in OSCTUNE<5:1> without affecting the INTRC frequency (see Register 2-1:OSCTUNE).**
- **If TUNSEL (OSCTUN2<7>) is set – The INTRC clock frequency can be adjusted by the TUN5:TUN1 bits in OSCTUN2<5:1> without affecting the INTOSC frequency (see Register 2-2: OSCTUN2).**

REGISTER 2-2: OSCTUN2: INTRC OSCILLATOR TUNING REGISTER values are modified. The modified content for bit 7 is indicated in bold text and the second sentence in bit 0 is deleted, and the modified content is indicated in bold text in Register 2-2.

REGISTER 2-2: OSCTUN2: INTRC OSCILLATOR TUNING REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TUNSEL	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **TUNSEL: INTRC Frequency bit**
1 = INTRC frequency adjusted according to the values of the OSCTUN2<5:1> bits
0 = INTRC not affected

bit 6 Unimplemented: Read as '0'

bit 5-1 TUN<5:1>: Frequency Tuning bits – Adjusts the frequency of INTRC when TUNSEL is set
011111 = Maximum frequency
•
•
000001
000000 = Center frequency. Oscillator module is running at the calibrated frequency
111111
•
•
100000 = Minimum frequency

bit 0 **TUN<0>: Placeholder. This bit has no effect on the INTRC frequency.**

4. Module: Electrical Characteristics (DC Power-Down and Supply Current)

Table 26.2: DC Characteristics: Power-Down and Supply Current, on page 317, is modified. The modified values – typical and maximum values for parameter D022A (Brown-out Reset), parameter D022B (Low-Voltage Detect), D025 (Timer1 Oscillator) and D026 (A/D Converter) – are indicated in bold text in the Table 26-2.

TABLE 26-2: DC Characteristics: Power-Down and Supply Current PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial) (Continued)

PIC18LF2220/2320/4220/4320 (Industrial)		**Standard Operating Conditions: (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial					
PIC18F2220/2320/4220/4320 (Industrial, Extended)		**Standard Operating Conditions: (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
D022 (ΔIWDT)	Module Differential Currents (ΔIWDT, ΔIBOR, ΔILVD, ΔIOSCB, ΔIAD)						
	Watchdog Timer	1.5	4.0	μA	-40°C	VDD = 2.0V	
		2.2	4.0	μA	+25°C		
		3.1	5.0	μA	+85°C		
		2.5	6.0	μA	-40°C	VDD = 3.0V	
		3.3	6.0	μA	+25°C		
		4.7	7.0	μA	+85°C		
		3.7	10.0	μA	-40°C	VDD = 5.0V	
		4.5	10.0	μA	+25°C		
		6.1	13.0	μA	+85°C		
D022A (ΔIBOR)	Brown-out Reset	35	50	μA	-40°C to +85°C	VDD = 3.0V	
		42	60	μA		VDD = 5.0V	
	Extended Devices Only	46	65	μA	-40°C to +125°C		
D022B (ΔILVD)	Low-Voltage Detect	31	45	μA	-40°C to +85°C	VDD = 2.0V	
		33	50	μA		VDD = 3.0V	
		42	60	μA		VDD = 5.0V	
	Extended Devices Only	46	65	μA	-40°C to +125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
MCLR = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

TABLE 26-2: DC Characteristics: Power-Down and Supply Current PIC18F2220/2320/4220/4320 (Industrial) PIC18LF2220/2320/4220/4320 (Industrial) (Continued)

PIC18LF2220/2320/4220/4320 (Industrial)		**Standard Operating Conditions: (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial					
PIC18F2220/2320/4220/4320 (Industrial, Extended)		**Standard Operating Conditions: (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial Operating temperature -40°C ≤ TA ≤ +125°C for extended					
Param No.	**Device**	**Typ**	**Max**	**Units**	**Conditions**		
D025 (ΔIOSCB)	Timer1 Oscillator	**1.7**	**3.5**	μA	-40°C	VDD = 2.0V	32 kHz on Timer1[(4)]
		1.8	**3.5**	μA	+25°C		
		2.1	**4.5**	μA	+85°C		
		2.2	**4.5**	μA	-40°C	VDD = 3.0V	32 kHz on Timer1[(4)]
		2.6	**4.5**	μA	+25°C		
		2.8	**5.5**	μA	+85°C		
		3.0	6.0	μA	-40°C	VDD = 5.0V	32 kHz on Timer1[(4)]
		3.3	**6.0**	μA	+25°C		
		3.4	7.0	μA	+85°C		
D026 (ΔIAD)	**A/D Converter**	**1.0**	**3.0**	μA	-40°C to +85°C	VDD = 2.0V	A/D on, not converting
		1.0	**4.0**	μA	-40°C to +85°C	VDD = 3.0V	
		2.0	**10.0**	μA	-40°C to +85°C	VDD = 5.0V	
		1.0	8.0	μA	-40°C to +125°C	VDD = 5.0V	

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.
The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD;
$\overline{\text{MCLR}}$ = VDD; WDT enabled/disabled as specified.

3: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be estimated by the formula Ir = VDD/2REXT (mA) with REXT in kΩ.

4: Standard low-cost 32 kHz crystals have an operating temperature range of -10°C to +70°C. Extended temperature crystals are available at a much higher cost.

REVISION HISTORY

Rev A Document (7/2007)

Initial release of this errata. Includes Data Sheet Clarifications 1 (Oscillator Configurations), 2 (Power-Managed Modes), 3-4 (I/O Ports), 5 (Comparator Voltage Reference Module) and 6 (Special Features of the CPU).

Rev B Document (6/2008)

Removed previous Data Sheet Clarifications 1-6. Added new Data Sheet Clarifications 1 (Power-Managed Modes), 2 (Oscillator Configurations – INTRC), 3 (OSCTUN2 Register) and 4 (Electrical Characteristics – DC Power-Down and Supply Current).

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