

Features

- Supports requirements of ITU-T G.8262 for Synchronous Ethernet Equipment Slave Clocks (EEC option 1 and 2)
- Supports requirements of Telcordia GR-1244 Stratum 3 and GR-253, ITU-T G.813, and G.781 SETS
- Supports ITU-T G.823, G.824 and G.8261 for 2048 kbit/s and 1544 kbit/s interfaces
- Programmable synthesizers generate any clock-rate from 1 Hz to 750 MHz
- Two precision synthesizers generate clocks with jitter below 0.8 ps RMS for 10 G PHYs
- Programmable digital PLL synchronize to any clock rate from 1 Hz to 750 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLL filter jitter from 0.1 mHz, 1 mHz, 10 mHz, 0.1 Hz, 1.7 Hz, 3.6 Hz, 7 Hz, 14 Hz,

Ordering Information

ZL30153GGG	100 Pin LBGA	Trays
ZL30153GGG2	100 Pin LBGA*	Trays

*Pb Free Tin/Silver/Copper
-40°C to +85°C

28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz

- Automatic hitless reference switching and digital holdover on reference fail
- Four reference inputs configurable as single ended or differential
- Eight LVPECL outputs and four LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI/I2C interface

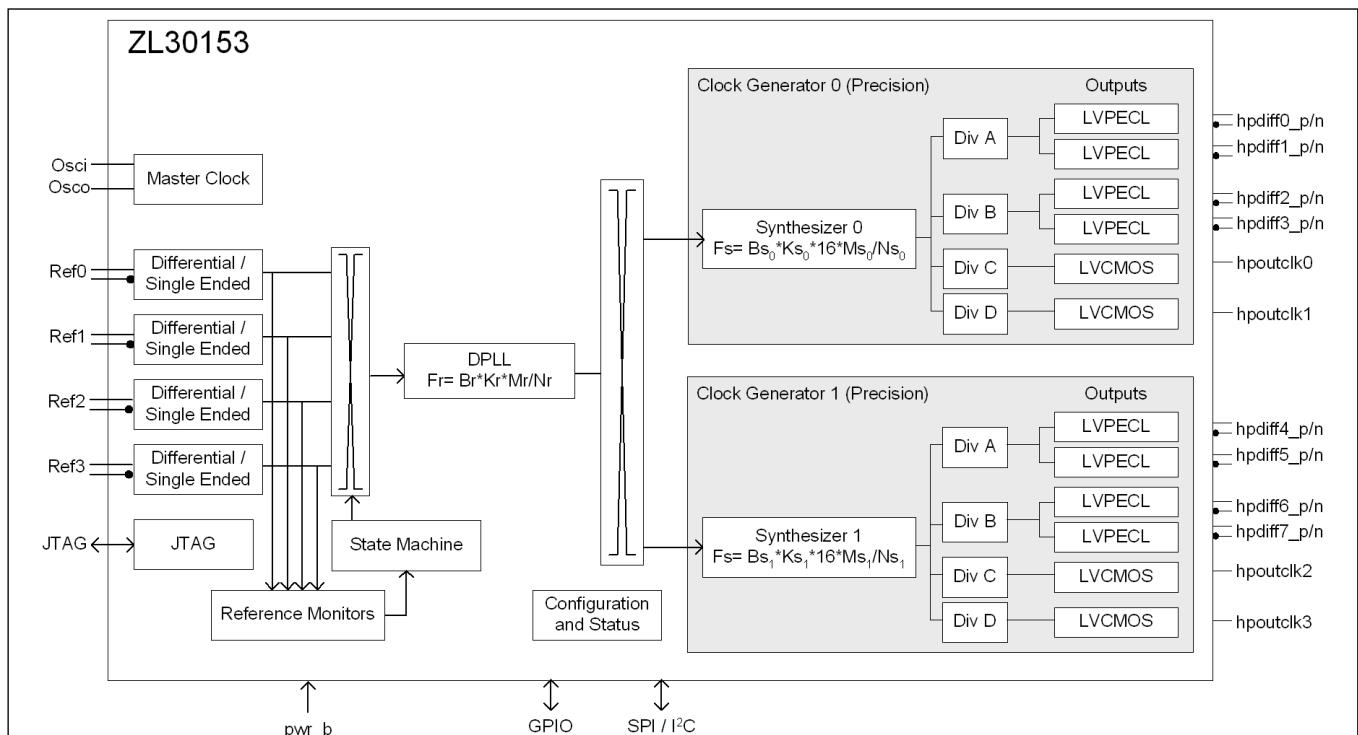
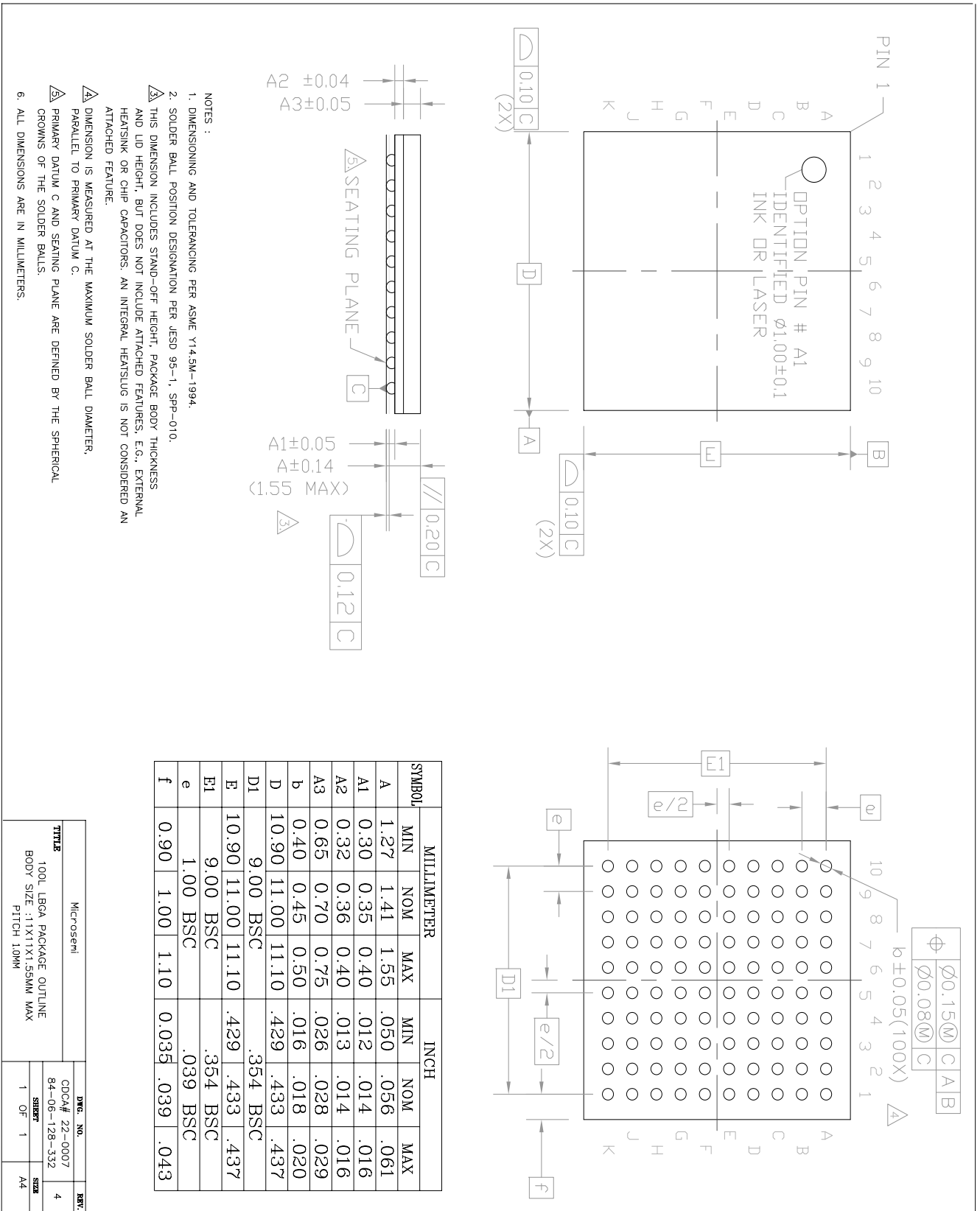


Figure 1 - Functional Block Diagram

Applications

- 10 Gigabit line cards
- Synchronous Ethernet, 10GBASE-R and 10GBASE-W
- OTN multiplexers and transponders
- SONET/SDH, Fibre Channel, XAUI

Mechanical Drawing



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.27	1.41	1.55	.050	.056	.061
A1	0.30	0.35	0.40	.012	.014	.016
A2	0.32	0.36	0.40	.013	.014	.016
A3	0.65	0.70	0.75	.026	.028	.029
b	0.40	0.45	0.50	.016	.018	.020
D	10.90	11.00	11.10	.429	.433	.437
D1	9.00	BSC		.354	BSC	
E	10.90	11.00	11.10	.429	.433	.437
E1	9.00	BSC		.354	BSC	
e	1.00	BSC		.039	BSC	
f	0.90	1.00	1.10	0.035	.039	.043

- NOTES :
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 2. SOLDER BALL POSITION DESIGNATION PER JE5D 95-1, SPP-010.
 3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
 4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
 5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
 6. ALL DIMENSIONS ARE IN MILLIMETERS.

Microsemi		DWG. NO.		REV.	
TTITLE		CDOCA# 22-0007		4	
100L TBGA PACKAGE OUTLINE		84-06-128-332		SHEET	
BODY SIZE :11X11X1.55MM MAX		PITCH 10MM		1 OF 1	
		DATE		A4	



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