MP2116

2A, 6V, 100% Duty Cycle Synchronous Step-Down Converter with 0.5A LDO

The Future of Analog IC Technology

DESCRIPTION

The MP2116 is an internally compensated 1.25MHz, 2A synchronous step-down switching DC-DC converter plus a standalone low-input voltage, 0.5A low dropout (LDO) linear regulator. It is ideal for powering portable equipment that operates from a single cell Lithium-Ion (Li+) Battery. The MP2116 can provide up to 2A to the switcher output, and 0.5A load current to the LDO output from a 2.5V to 6V input voltage. Both output voltages can be regulated as low as 0.6V.

The 2A Synchronous switcher features integrated high-side and low-side switch for high efficiency and small footprint. With peak current mode control and internal compensation, the MP2116 is stable with ceramic capacitors. Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The standalone low-input voltage 0.5A LDO is used to power noise sensitive circuitry. The LDO's separate input supply pin (IN2) can be connected to the switcher output to reduce power dissipation and noise from the main switcher.

MP2116 is available in the small 10-pin 3mmx3mm QFN package.

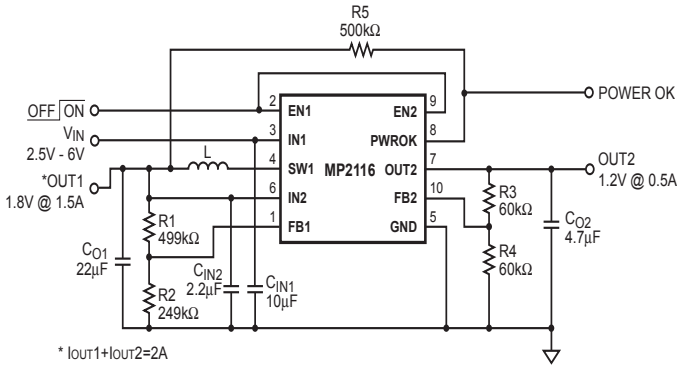
FEATURES

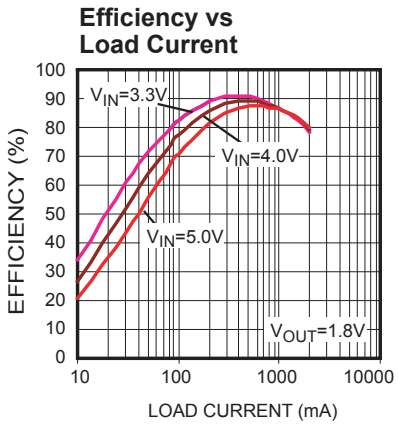
- 100% Duty Cycle Low Dropout Operation (High-Side PFET)
- 2A Switcher Output Current at V_{IN}=3V
- Internal Power MOSFET Switches
- Stable with Ceramic Capacitors
- Up to 95% Efficiency for Switcher
- 1.25MHz Switching Frequency
- Internal Soft-start for Switcher
- 2.5V to 6V Input Range, for Switcher
- 1V to V_{IN1} Input Range, for LDO
- 0.5A LDO Output Current
- 1μA Shutdown Current
- Thermal Shutdown
- Cycle-by-Cycle Over Current Protection
- Short Circuit Protection
- Power OK Output
- Available in 10-Pin QFN Package

APPLICATIONS

- DVD+/-RW Drives
- Smart Phones
- PDAs
- Digital Cameras
- Portable Instruments

TYPICAL APPLICATION





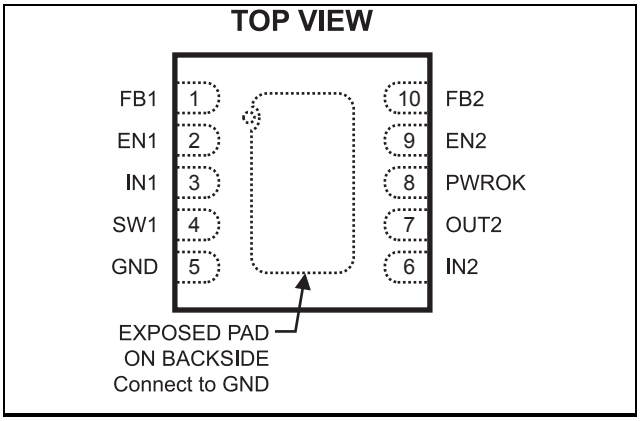
ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP2116DQ	QFN10 (3mm x 3mm)	P4	–40°C to +85°C

For Tape & Reel, add suffix –Z (eg. MP2116DQ–Z)

For Lead Free, add suffix –LF (EG. MP2116DQ–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

IN1, OUT1/2 to GND .....–0.3V to + 6.5V
IN2 to GND .....–0.3V to V_{IN1} + 0.3V
SW1 to GND .....–0.3V to V_{IN1} + 0.3V
.....(-2.5V<V_{SW1}<+8.5V Transient <50ns)
PWROK to GND .....–0.3V to +6.5V
FB1/2, EN1/2 to GND .....–0.3V to +6.5V
Operating Temperature..... –40°C to +85°C
Continuous Power Dissipation (T_A = +25°C)(2)
…….2.5W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature ..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN1}.....2.5V to 6V
Supply Voltage V_{IN2}..... 1.0V to V_{IN1}
Output Voltage $V_{OUT\_}$ .....0.6V to 6V
Operating Temperature..... –40°C to +85°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN10 (3mm x 3mm) .....50 ..... 12 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on approximately 1” square of 1 oz copper.

ELECTRICAL CHARACTERISTICS (5)

$V_{IN1/2}$ = $V_{EN1/2}$ = 3.6V, T_A = +25°C, unless otherwise noted.

Parameters	Condition	Min	Typ	Max	Units
No Load Supply Current	$V_{IN1/2}$ = 3.6V, V_{EN1}=3.6V, V_{EN2}=0V V_{FB1} = 0.58V		300	500	µA
	$V_{IN1/2}$ = 3.6V, V_{EN1}=0V, V_{EN2}=3.6V V_{FB2} = 0.62V		70	120	
Shutdown Current	$V_{EN1/2}$ = 0V, $V_{IN1/2}$ = 6V		0.01	1	µA
Thermal Shutdown Trip Threshold	Hysteresis = 20°C		150		°C
PWROK Upper Trip Threshold	FB1/2 with respect to the Nominal Value		10		%
PWROK Lower Trip Threshold	FB1/2 with respect to the Nominal Value		–10		%
PWROK Output Lower Voltage	I_{SINK} = 5mA			0.3	V
PWROK Deglitch Timer (FB1)	Switching Regulator		50		µs
PWROK Deglitch Timer (FB2)	LDO		150		
EN1/2 Trip Threshold	–40°C ≤ T_A ≤ +85°C	0.3	0.96	1.5	V
EN1/2 Pull Down Resistor			1		MΩ
Switching Regulator					
IN1 Under Voltage Lockout Threshold	Rising Edge, Hysteresis=0.3V	1.90	2.15	2.40	V
Regulated FB1Voltage	T_A = +25°C	0.588	0.600	0.612	V
	–40°C ≤ T_A ≤ +85°C	0.582	0.600	0.618	
FB1 Input Bias Current	V_{FB1} = 0.62V	–50	–2	+50	nA
SW1 PFET On Resistance	I_{SW1} = 100mA		0.20		Ω
SW1 NFET On Resistance	I_{SW1} = –100mA		0.15		Ω
SW1 Leakage Current	V_{EN} = 0V, V_{IN} = 6V V_{SW} = 0V or 6V	–5		+5	µA
SW1 PFET Peak Current Limit	Duty Cycle = 100%, Current Pulse Width < 1ms	2.2	3.1	4.0	A
Oscillator Frequency		1.00	1.25	1.50	MHz
Linear Regulator LDO					
IN2 Input Range	I_{LOAD2} = 10mA, V_{OUT2}=V_{FB2}	1		V_{IN1}	V
Regulated FB2 Voltage	T_A = +25°C	0.588	0.600	0.612	V
	–40°C ≤ T_A ≤ +85°C	0.582	0.600	0.618	
FB2 Input Bias Current	V_{FB2} = 0.6V	–50	–2	+50	nA
OUT2 Maximum Output Current	V_{OUT2} = 1.2V	500	-		mA
OUT2 Current Limit	V_{OUT2} = 0V	600	700		mA
Dropout Voltage	I_{LOAD} = 0.15A, V_{OUT2} = 1.2V		100		mV

Notes:

5) Production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.

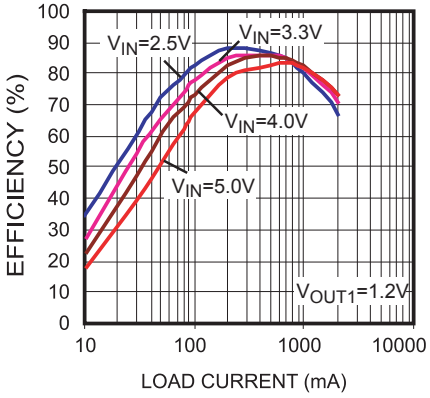
PIN FUNCTIONS

Pin #	Name	Description
1	FB1	Feedback Input for the switcher output VOUT1.
2	EN1	Enable Input for the switcher.
3	IN1	Main Input Supply Pin. Input supply for both the switcher and the low dropout (LDO) linear regulator, except the LDO output power device.
4	SW1	Switch node of the switcher.
5	GND (Exposed Pad)	Ground. Exposed pad must be connected to GND pin.
6	IN2	Input Supply for the linear regulator LDO output power device. Bypass with a 2.2uF from IN2 to GND.
7	OUT2	Output of the 500mA LDO. The LDO is designed to be stable with an external 4.7μF ceramic capacitor (minimum).
8	PWROK	Power OK Open Drain Output. HIGH output indicates that both outputs are within ±10% of the regulation value. LOW output indicates that the output is out of ±10% window. PWROK is pulled down in shutdown. The PWROK window comparators have 50μs deglitch timer for the switcher and 150μs deglitch timer for the linear regulator LDO to avoid false trigger during load transient.
9	EN2	Enable Input for the low-dropout LDO
10	FB2	Feedback Input for the LDO output VOUT2.

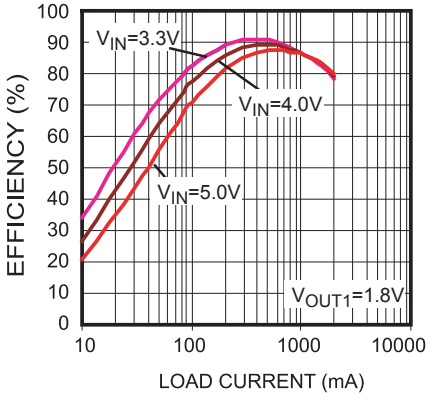
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=3.6V, V_{OUT1}=1.8V, V_{OUT2}=1.2V, C_{IN1}=10uF, C_{O1}=22uF, C_{IN2}=2.2uF, C_{O2}=4.7uF, L=1uH, T_A=25ºC, unless otherwise noted.

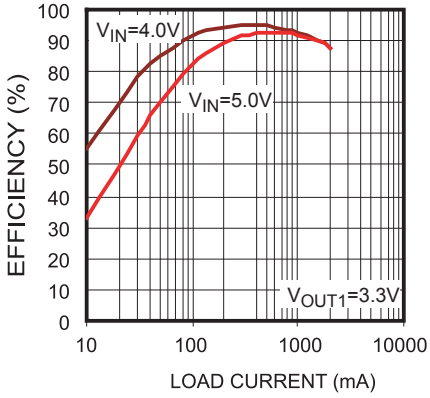
Switcher Efficiency vs Load Current



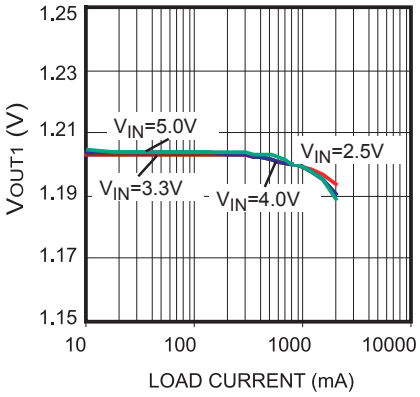
Switcher Efficiency vs Load Current



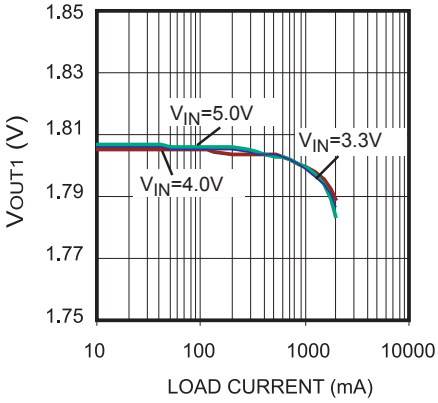
Switcher Efficiency vs Load Current



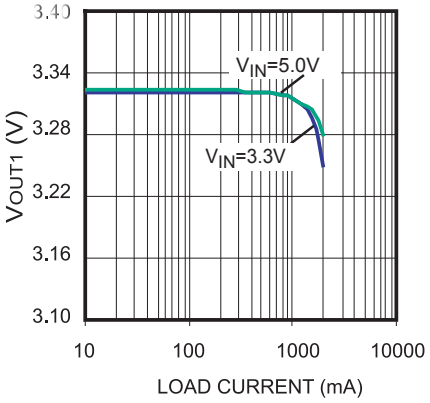
Switcher Output Voltage vs Load Current



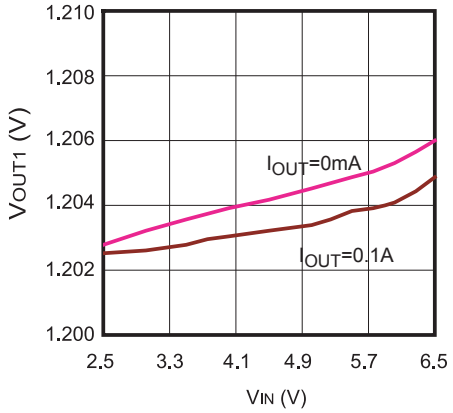
Switcher Output Voltage vs Load Current



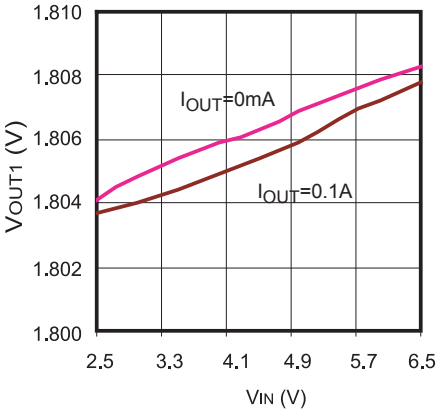
Switcher Output Voltage vs Load Current



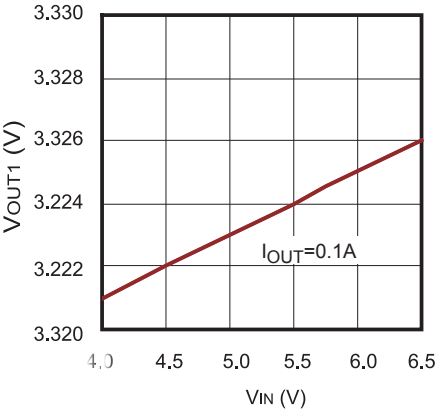
Switcher Output Voltage vs Input Voltage



Switcher Output Voltage vs Input Voltage



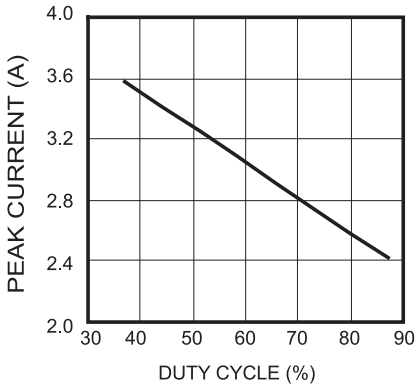
Switcher Output Voltage vs Input Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

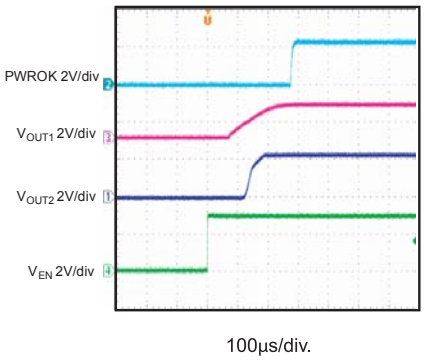
V_{IN}=3.6V, V_{OUT1}=1.8V, V_{OUT2}=1.2V, C_{IN1}=10uF, C_{O1}=22uF, C_{IN2}=2.2uF, C_{O2}=4.7uF, L=1uH, T_A=25ºC, unless otherwise noted.

Peak Current vs Duty Cycle



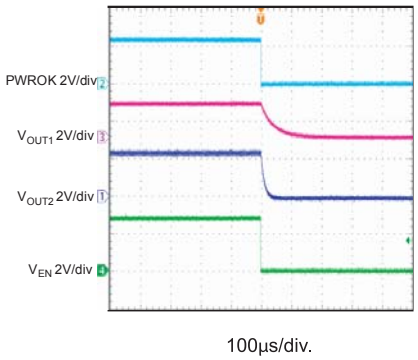
Enable Turn On

V_{IN1}=2.6V, V_{EN}=EN1=EN2=3V, V_{IN2}=V_{OUT1}, I_{O1}=0.1A, I_{O2}=0.5A with Resistor load

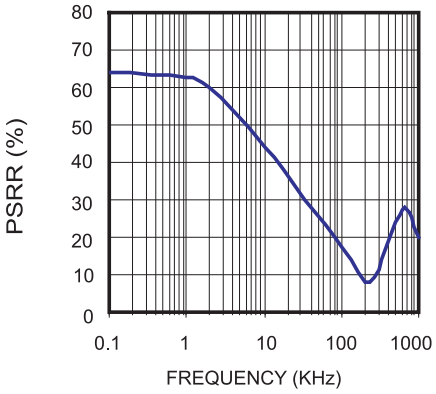


Enable Turn Off

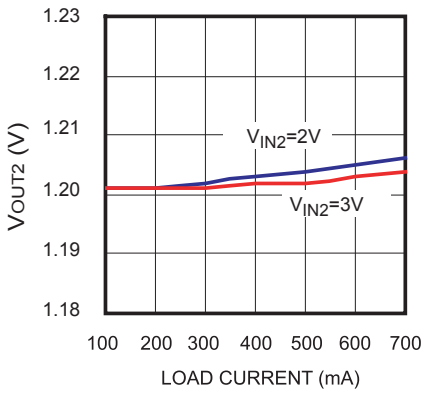
V_{IN1}=2.6V, V_{EN}=EN1=EN2=3V, V_{IN2}=V_{OUT1}, I_{O1}=0.1A, I_{O2}=0.5A with Resistor load



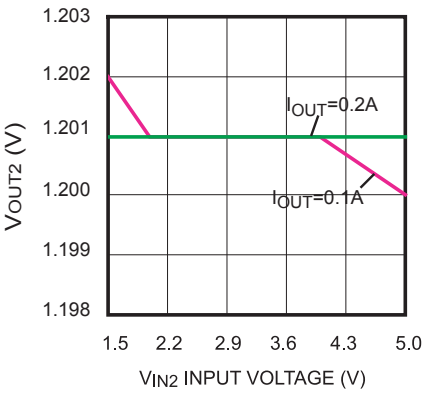
LDO PSRR vs FREQUENCY



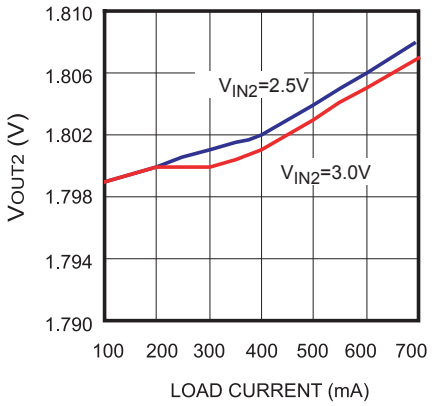
LDO OUTPUT VOLTAGE vs LOAD CURRENT



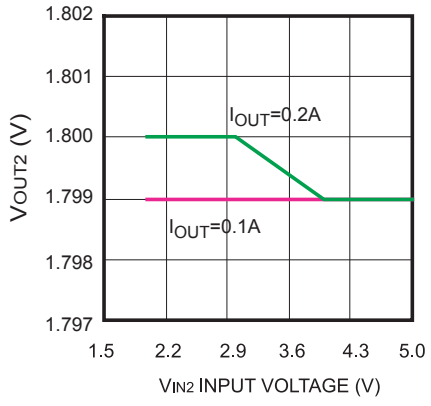
LDO OUTPUT VOLTAGE vs INPUT VOLTAGE



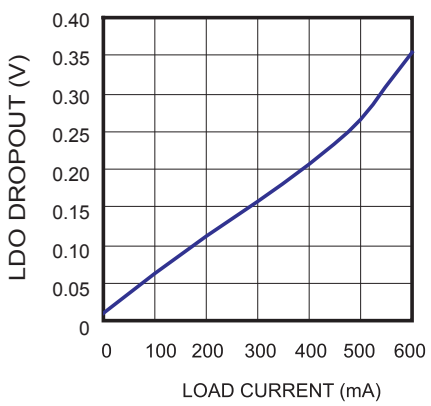
LDO OUTPUT VOLTAGE vs LOAD CURRENT



LDO OUTPUT VOLTAGE vs INPUT VOLTAGE



LDO DROPOUT vs LOAD CURRENT

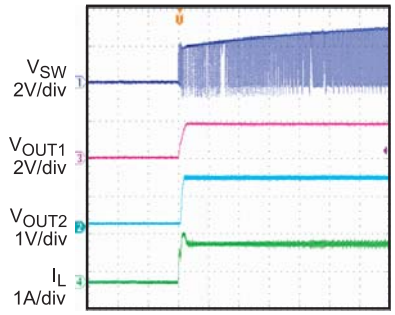


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=3.6V, V_{OUT1}=1.8V, V_{OUT2}=1.2V, C_{IN1}=10uF, C_{O1}=22uF, C_{IN2}=2.2uF, C_{O2}=4.7uF, L=1uH, T_A=25ºC, unless otherwise noted.

V_{IN} Ramp Up

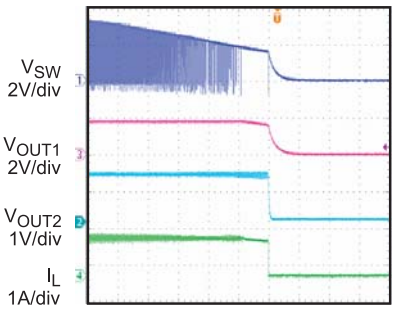
V_{OUT1}=V_{IN2}=1.8V, EN1=EN2=V_{IN},
I_{O1}=I_{O2}=0.5A
with Resistor Load



400µs/div.

V_{IN} Ramp Down

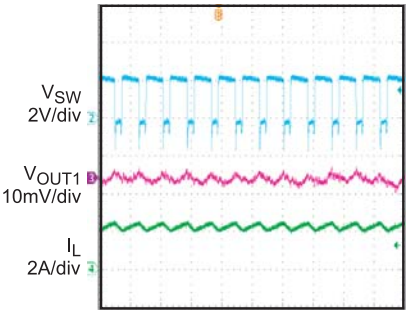
V_{OUT1}=V_{IN2}=1.8V, EN1=EN2=V_{IN},
I_{O1}=I_{O2}=0.5A
with Resistor Load



400µs/div.

Heavy Load Ripple

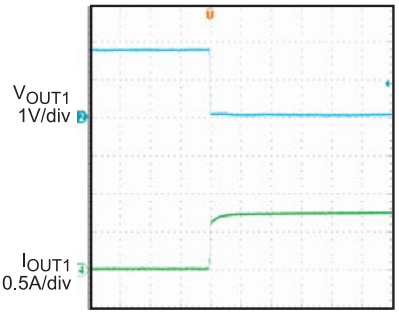
V_{IN}=2.5V, V_{OUT1}=1.2V
V_{EN}=V_{IN}, I_{O1}=2.2A



1µs/div.

V_{OUT1} Short Circuit

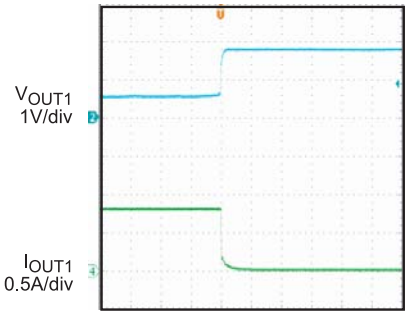
V_{EN1}=V_{IN1}=3.3V, V_{OUT1}=1.8V



400µs/div.

V_{OUT1} Short Circuit Recovery

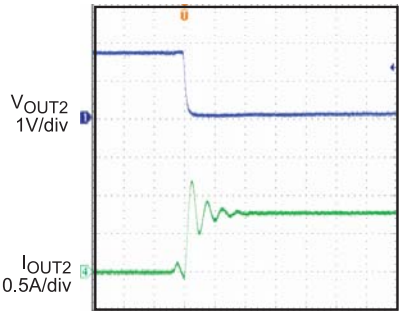
V_{EN1}=V_{IN1}=3.3V, V_{OUT1}=1.8V



400µs/div.

V_{OUT2} Short Circuit

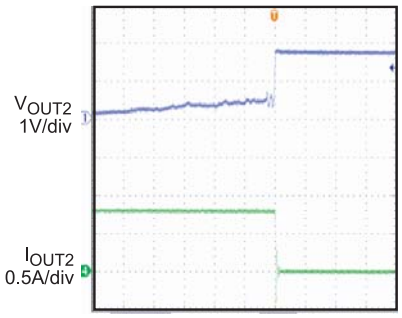
V_{IN2}=3.6V, V_{OUT2}=1.8V



20µs/div.

V_{OUT2} Short Circuit Recovery

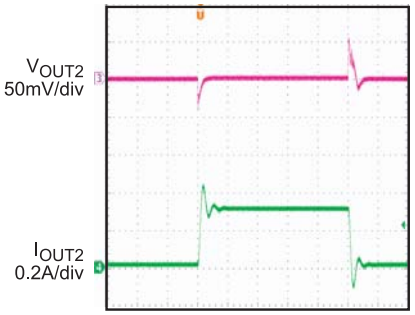
V_{IN2}=3.6V, V_{OUT2}=1.8V



200µs/div.

LDO Load Transient

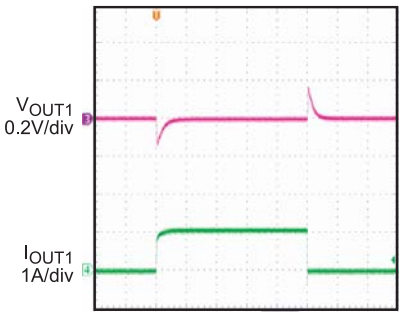
V_{IN2}=2.6V, V_{OUT2}=1.2V
I_{OUT2}=10mA to 310mA
with Resistor Load



100µs/div.

Switcher Load Transient

V_{IN1}=2.5V, V_{OUT1}=1.2V
I_{OUT1}=0 to 1A
with Resistor Load



100µs/div.

TYPICAL PERFORMANCE CHARACTERISTICS

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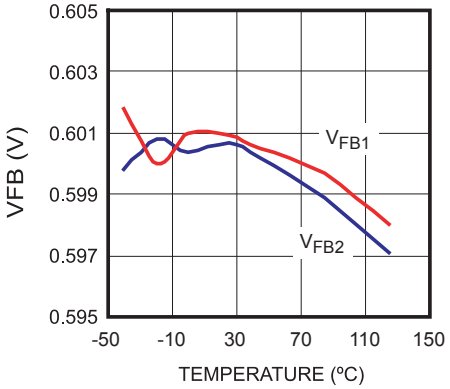
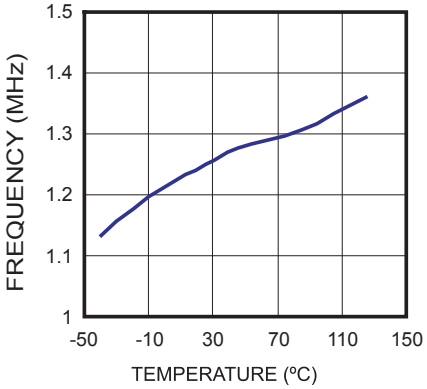
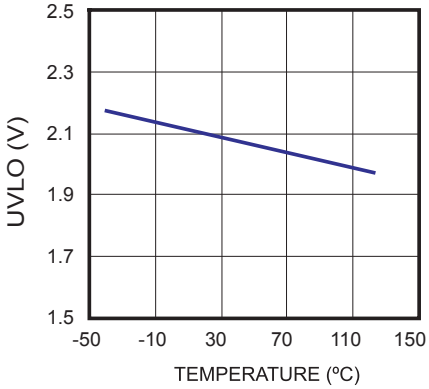
V_{FB} vs. TEMPERATURE



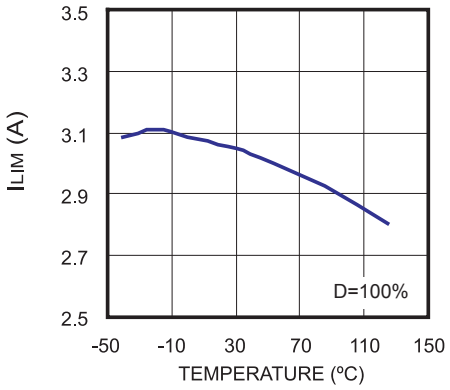
FREQUENCY vs. TEMPERATURE



V_{IN1} UVLO vs. TEMPERATURE



PFET CURRENT LIMIT vs. TEMPERATURE



OPERATION

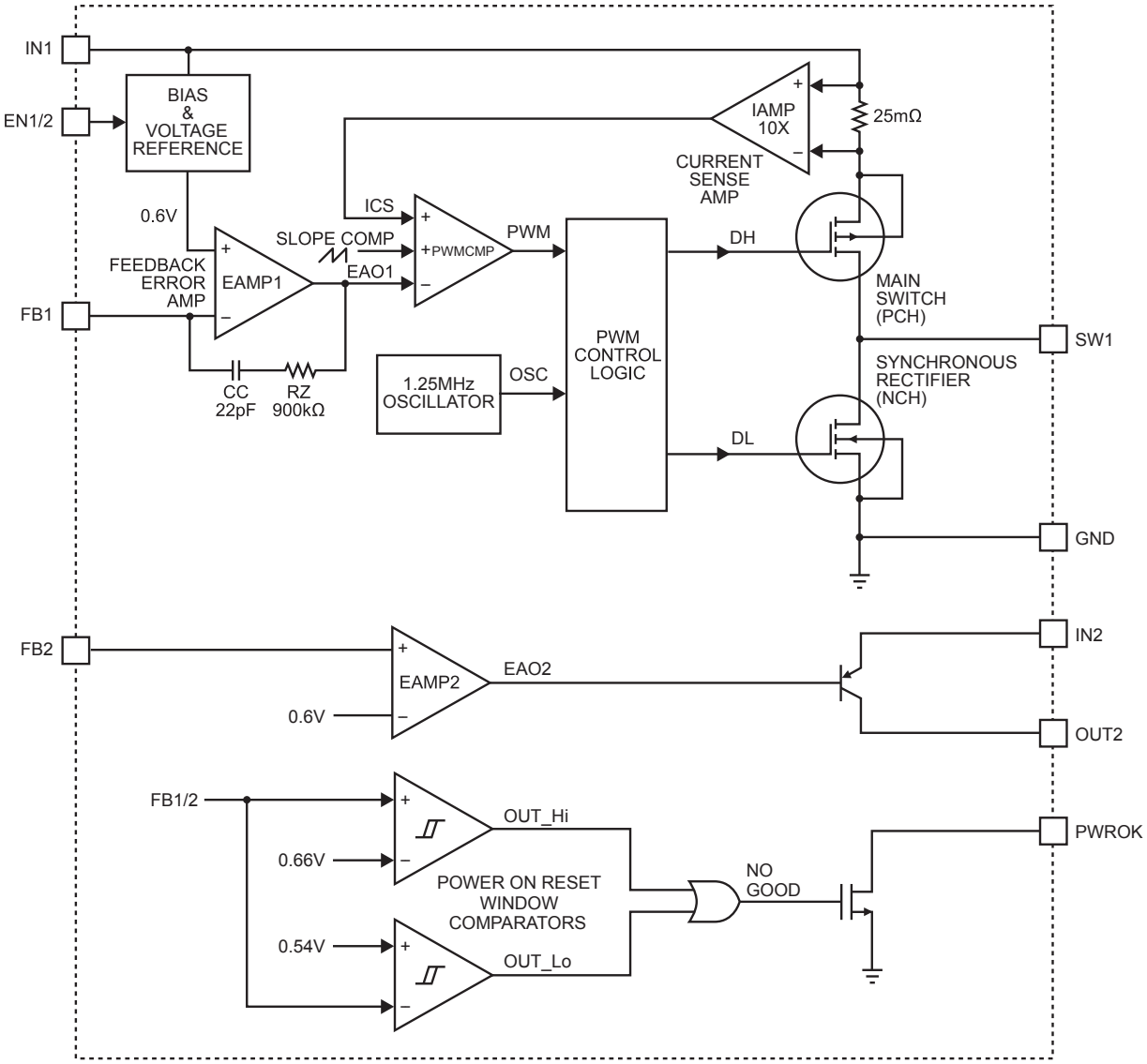


Figure1—MP2116 Functional Block Diagramm

The MP2116 is a 1.25MHz current mode 2A synchronous step-down switcher plus a low input 0.5A low dropout (LDO) linear regulator (see Figure1). The MP2116 is optimized for low voltage, Li-Ion battery powered applications where high efficiency and small size are critical.

The MP2116 uses an external resistor divider to set both the switcher and LDO output voltage from 0.6V to 6V.

2A Synchronous Step-Down Switcher

The switcher integrates both a main switch and a synchronous rectifier, which provides high efficiency and eliminates an external Schottky diode.

The duty cycle D of a step-down switcher is defined as:

$$D = T_{ON} \times f_{OSC} \times 100\% \approx \frac{V_{OUT}}{V_{IN}} \times 100\%$$

Where T_{ON} is the main switch on time and f_{OSC} is the oscillator frequency (1.25MHz).

Current Mode PWM Control

Slope compensated current mode PWM control provides stable switching and cycle-by-cycle current limiting for superior load and line response in addition to protection of the internal main switch and synchronous rectifier. The MP2116 switches at a constant frequency (1.25MHz) and regulates the output voltage. During each cycle the PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage. During normal operation, the main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator, and switched off when the peak inductor current is above the error voltage. When the main switch is off, the synchronous rectifier will be turned on immediately and stay on until the next cycle starts.

Dropout Operation

The MP2116 allows the main switch to remain on for more than one switching cycle and increases the duty cycle while the input voltage is dropping close to the output voltage. When the duty cycle reaches 100%, the main switch is held on continuously to deliver current to the output up to the PFET current limit. The output voltage then becomes the input voltage minus the voltage drop across the main switch and the inductor.

Short Circuit Protection

When the output is shorted to ground, the oscillator frequency is reduced to prevent the inductor current from increasing beyond the PFET current limit. The PFET current limit is also reduced to lower the short circuit current. The frequency and current limit will return to the normal values once the short circuit condition is removed and the feedback voltage reaches 0.6V.

Maximum Switcher Output Current

The MP2116 switcher can provide up to 2A output current, and operate down to 3V input voltage; however the maximum output current decreases at lower input voltage due to a large IR drop on the main switch and synchronous rectifier. The slope compensation signal reduces the peak inductor current as a function of the duty cycle to prevent sub-harmonic oscillations at duty cycles greater than 50%. Conversely, the current limit increases as the duty cycle decreases

Power OK

The MP2116 provides an open-drain PWROK output that goes high after both channels reach regulation during startup. PWROK goes low after one of the output channels goes out of regulation by ±10% or when device enters shutdown. There are deglitch timers built in to avoid PWROK false triggered during load transient: 50μS for the switcher and 150μS for the LDO.

Low Input 0.5A Linear Regulator

The low input 0.5A low dropout (LDO) linear regulator has separate input IN2 and output OUT2 pins for the internal power PNP device. The control circuitry of the LDO takes power from the main input supply IN1. Both IN1 and IN2 input supplies must be presented for the LDO working properly. The LDO power device input IN2 can be connected to the switcher output (Figure1) or directly to the main supply IN1 (Figure3). If the IN2 tied to the IN1, it is optional to insert a RC filter between IN1 and IN2. The RC filter will reduce switching noise coupling from IN1 to IN2 and power dissipation inside the MP2116

APPLICATION INFORMATION

Output Voltage Setting

The external resistor divider sets the output voltage. The feedback resistor R1 of the switcher also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure1).

Choose R1 feedback resistor of the switcher between 450kΩ and 800kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT1}}{0.6V} - 1}$$

See Table1 for recommended R1 & R2 resistor values.

Choose R4 of the LDO between 10kΩ and 100kΩ. R3 is then given by:

$$R3 = R4 \times (\frac{V_{OUT2}}{0.6V} - 1)$$

Table 1—Resistor Selection vs. Output Voltage Setting

V_{OUT}	R1	R2
1.2V	499kΩ (1%)	499kΩ (1%)
1.5V	499kΩ (1%)	332kΩ (1%)
1.8V	499kΩ (1%)	249kΩ (1%)
2.5V	499kΩ (1%)	158kΩ (1%)

Inductor Selection

A 1μH to 10μH inductor with DC current rating at least 25% higher than the maximum load current is recommended for most applications. For best efficiency, the inductor DC resistance shall be <100mΩ. See Table 2 for recommended inductors and manufacturers. For most designs, the inductance value can be derived from the following equation:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is inductor ripple current. Choose inductor ripple current approximately 30% of the maximum load current, up to 2A.

The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

Switcher Input Capacitor C_{IN1} Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency shall be less than input source impedance to prevent high frequency switching current passing to the input. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10μF~22μF capacitor is sufficient.

Switcher Output Capacitor C_{O1} Selection

The output capacitor keeps output voltage ripple small and ensures regulation loop stable. The output capacitor impedance shall be low at the switching frequency. Ceramic capacitors with X5R or X7R dielectrics are recommended. For most applications, a 22μF~47μF capacitor is sufficient.

The output ripple ΔV_{OUT} is approximately:

$$\Delta V_{OUT1} \le \frac{V_{OUT1} \times (V_{IN1} - V_{OUT1})}{V_{IN1} \times f_{OSC} \times L} \times \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{O1}} \right)$$

Table 2—Suggested Surface Mount Inductors

Manufacturer	Part Number	Inductance (uH)	Max DCR (mΩ)	Saturation Current (A)	Dimensions L x W x H (mm3)
TOKO	D62LCB	1.0	17	3.5	6.2 X6.3 X 2.0
SUMIDA	CDRH4D28C	1.0	17.5	3.0	5.1 X 5.1 X 3
DELTA	SIL525-1R0	1.0	38	3.2	5.0 X 5.0 X 2.5

Thermal Dissipation

Power dissipation shall be considered when both channels of the MP2116 provide maximum 2A switcher output current and 0.5A LDO output current to the loads at high ambient temperature. If the junction temperature rises above 150°C, the MP2116 two channels will be shut down.

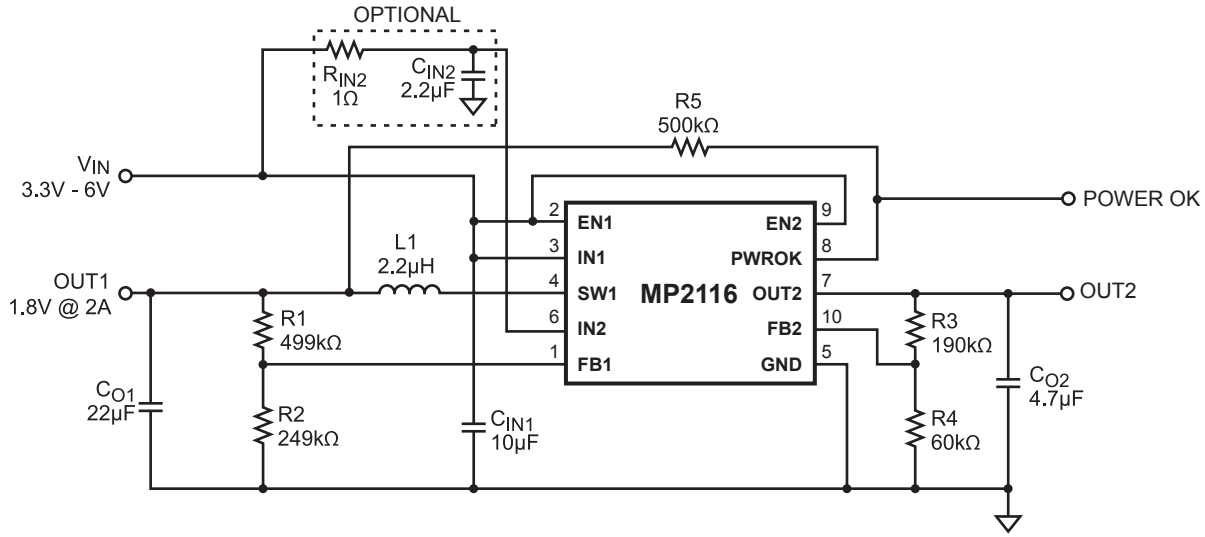
The junction-to-ambient thermal resistance of the 10-pin QFN (3mm x 3mm) $R_{\Theta JA}$ is 50°C/W. The maximum power dissipation is about 1.6W when the MP2116 is operating in a 70°C ambient temperature environment.

$$PD_{MAX} = \frac{150^{o}C - 70^{o}C}{50^{o}C/W} = 1.6W$$

PC Board Layout

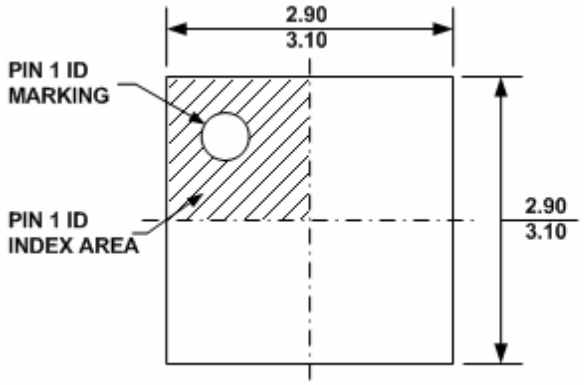
The high current paths (GND, IN1/IN2 and SW1) should be placed very close to the device with short, direct and wide traces. Input capacitors should be placed as close as possible to the respective IN and GND pins. The external feedback resistors shall be placed next to the FB pins. Keep the switching nodes SW1 short and away from the feedback network

TYPICAL APPLICATION CIRCUITS

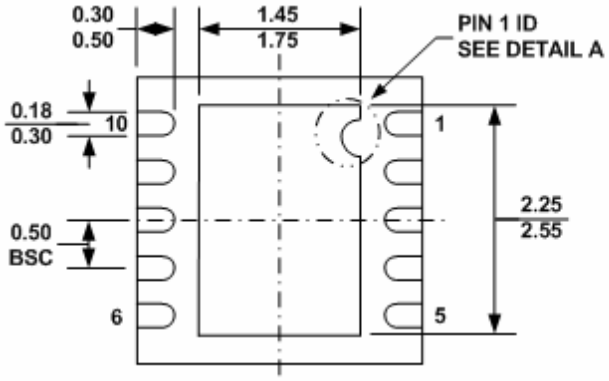


PACKAGE INFORMATION

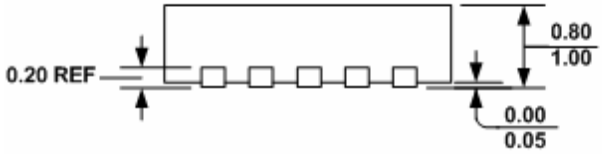
(3mmx3mm) QFN10



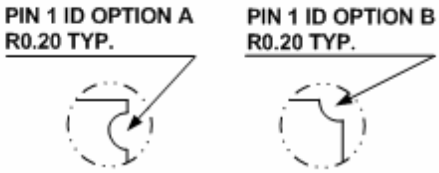
TOP VIEW



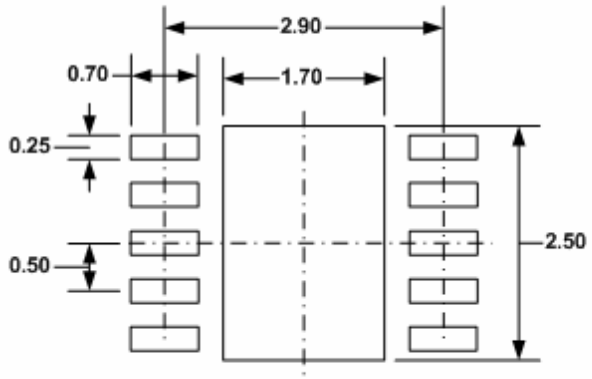
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-229, VARIATION VEED-5.
5) DRAWING IS NOT TO SCALE.