STD45NF75

N-channel 75 V, 0.018 Ω, 40 A DPAK STripFET™ II Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D
STD45NF75	75 V	< 0.024 Ω	40 A[1]

1. Current limited by package

- 100% avalanche tested
- Gate charge minimized

Application

- Switching applications

Description

This Power MOSFET is the latest development of STMicroelectronics's unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.
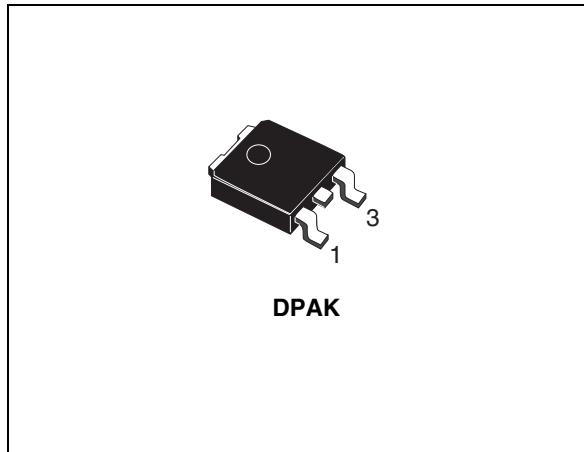

DPAK

Figure 1.   Internal schematic diagram

AM01474v1
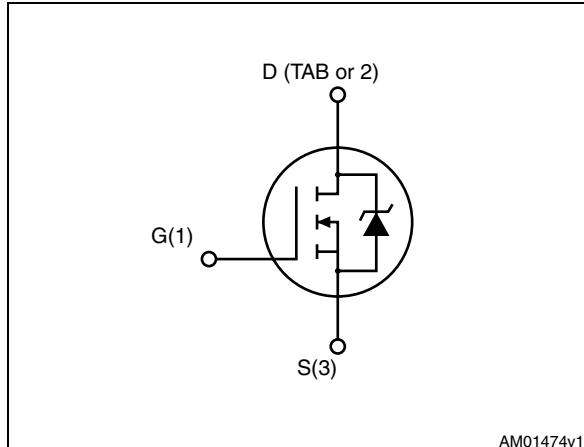
Table 1.   Device summary

Order code	Marking	Package	Packaging
STD45NF75T4	D45NF75	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2.   **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	75	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	75	V
V_{GS}	Gate- source voltage	± 20	V
I_D[1]	Drain current (continuous) at $T_C = 25 \,°C$	40	A
I_D	Drain current (continuous) at $T_C = 100 \,°C$	30	A
I_{DM}[2]	Drain current (pulsed)	160	A
P_{tot}	Total dissipation at $T_C = 25 \,°C$	125	W
	Derating factor	0.83	W/°C
dv/dt [3]	Peak diode recovery voltage slope	20	V/ns
E_{AS} [4]	Single pulse avalanche energy	500	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Current limited by package

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 40$ A, di/dt ≤ 800 A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

4. Starting $T_j = 25\,°C$, $I_D = 20$ A, $V_{DD} = 40$ V

Table 3.   **Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.2	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max	see *Figure 16.* and *Figure 17.*	°C/W
T_J	Maximum lead temperature for soldering purpose[1]	260	°C

1. for 10 sec. 1.6 mm from case

2 Electrical characteristics

(T_{CASE}=25 °C unless otherwise specified)

Table 4.   On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 μA, V_{GS} =0	75			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C = 125 °C			1 10	μA μA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 20 A		0.018	0.024	Ω

Table 5.   Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} [1]	Forward transconductance	V_{DS} = 25 V, I_D = 20 A	-	50		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	1760 360 140		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 37 V, I_D = 20 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 20*)	-	15 40 55 12		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 60 V, I_D = 40 A, V_{GS} = 10 V, R_G = 4.7 Ω (see *Figure 21*)	-	60 13 23	80	nC nC nC

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%.

Table 6.   Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} [1]	Source-drain current Source-drain current (pulsed)		-		40 160	A A
V_{SD} [2]	Forward on voltage	I_{SD} = 40 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40 A, V_{DD} = 30 V, di/dt = 100 A/µs, T_j = 150 °C (see *Figure 22*)	-	120 410 7.5		ns nC A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area
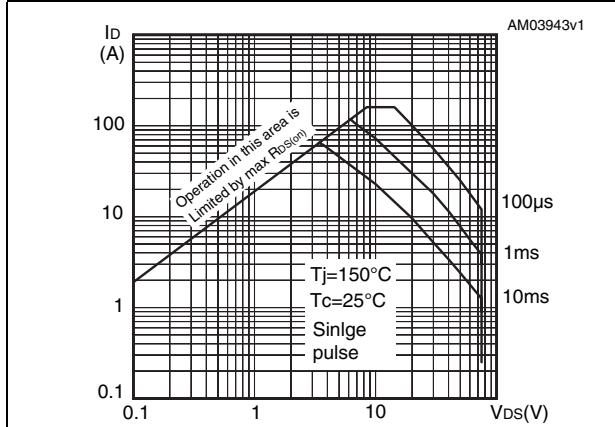
Figure 3. Thermal impedance
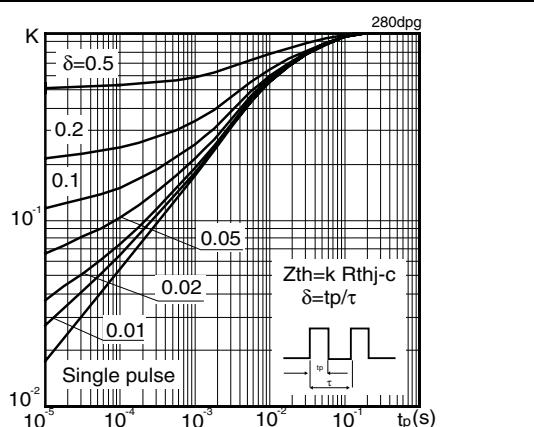
Figure 4. Output characteristics
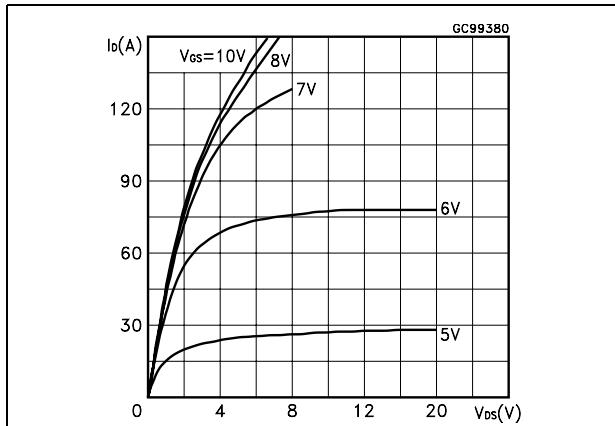
Figure 5. Transfer characteristics
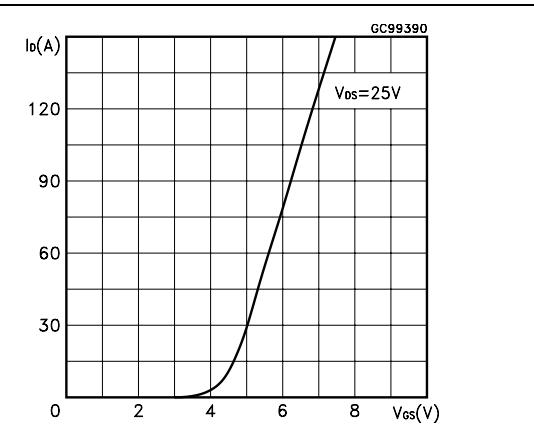

**Figure 6.** Transconductance
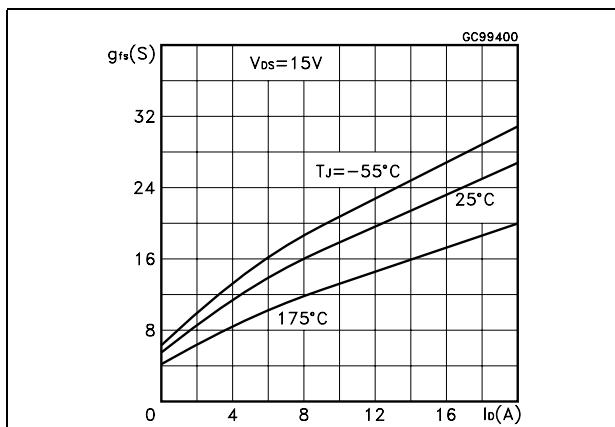
**Figure 7.** Static drain-source on resistance
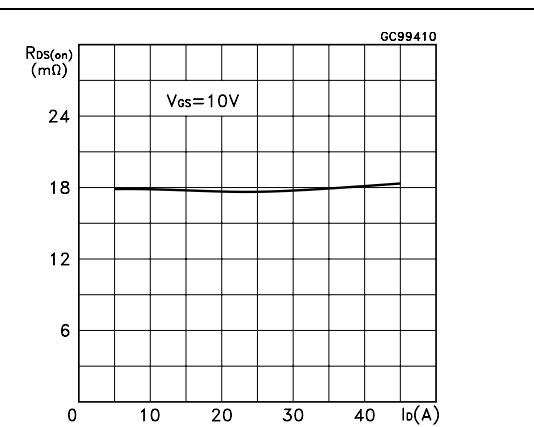
Figure 8. **Gate charge vs. gate-source voltage**
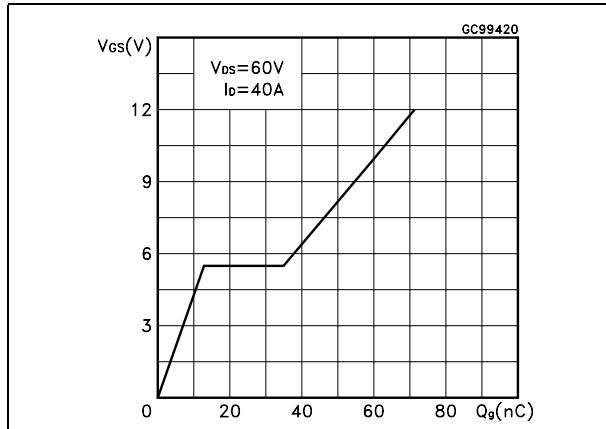

**Figure 9.** **Capacitance variations**
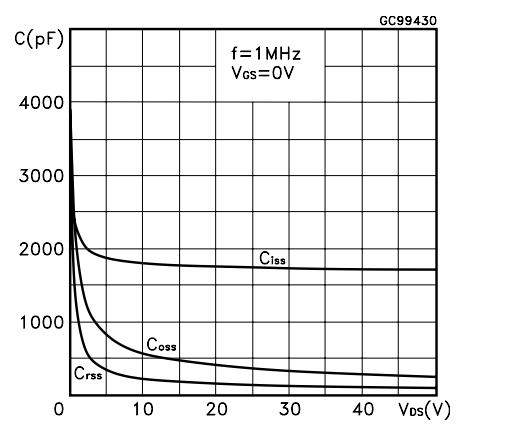
Figure 10. **Normalized gate threshold voltage vs. temperature**
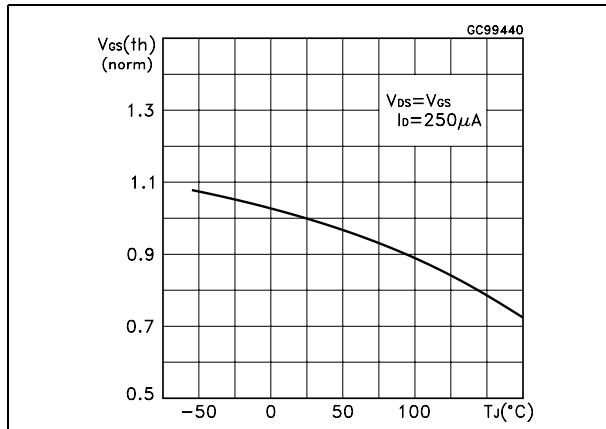

**Figure 11.** **Normalized on resistance vs. temperature**
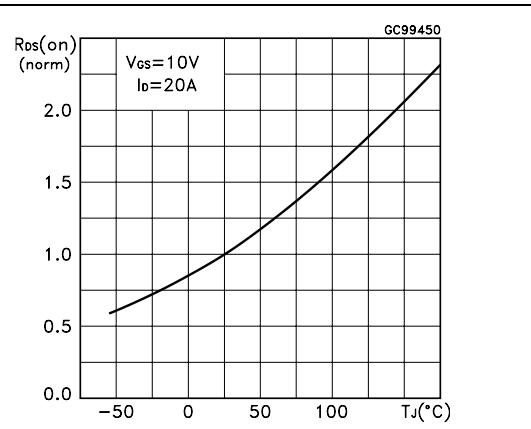
**Figure 12.** **Source-drain diode forward characteristics**
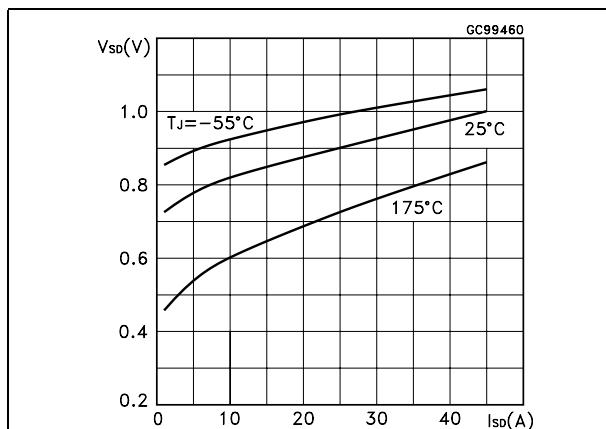
**Figure 13.** **Normalized breakdown voltage vs. temperature**
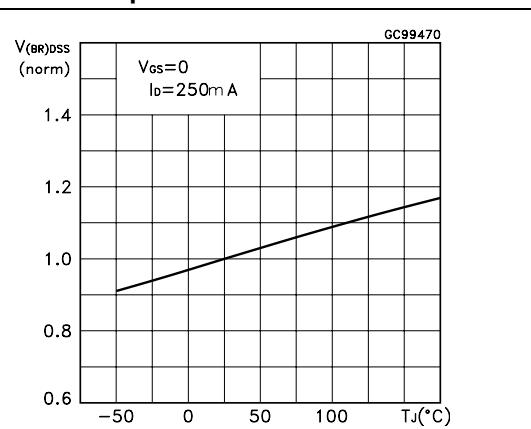
**Figure 14. Power derating vs. Tj**
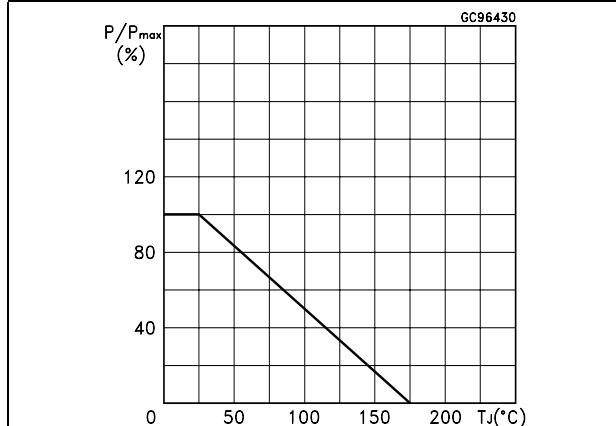
**Figure 15. Max Id current vs. Tc**
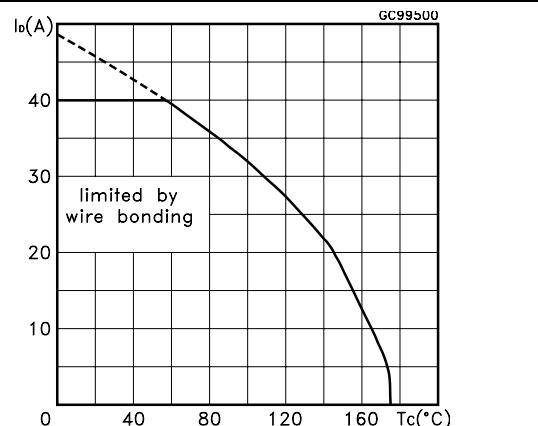
**Figure 16. Thermal resistance Rthj-a vs. pcb copper area**
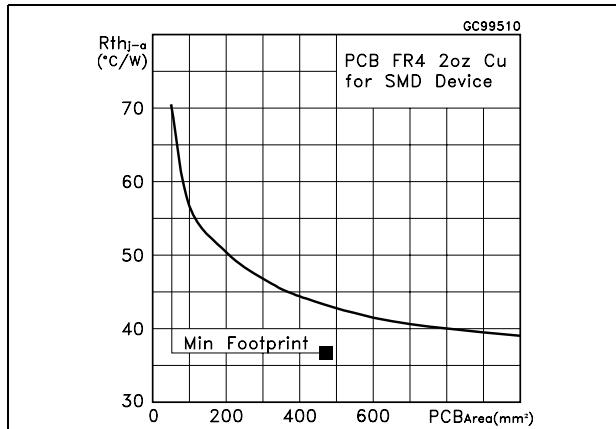
Figure 17. Max power dissipation vs. pcb copper area
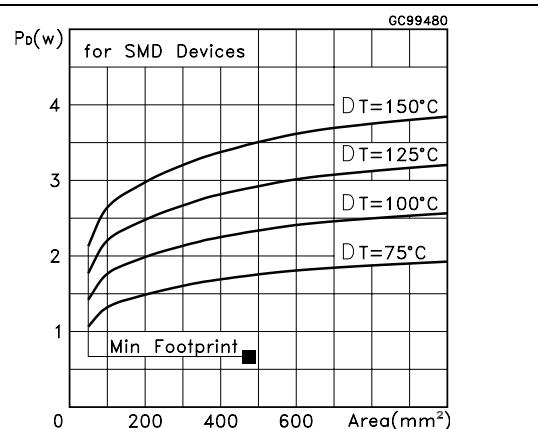
Figure 18.   Allowable Iav vs. time in avalanche
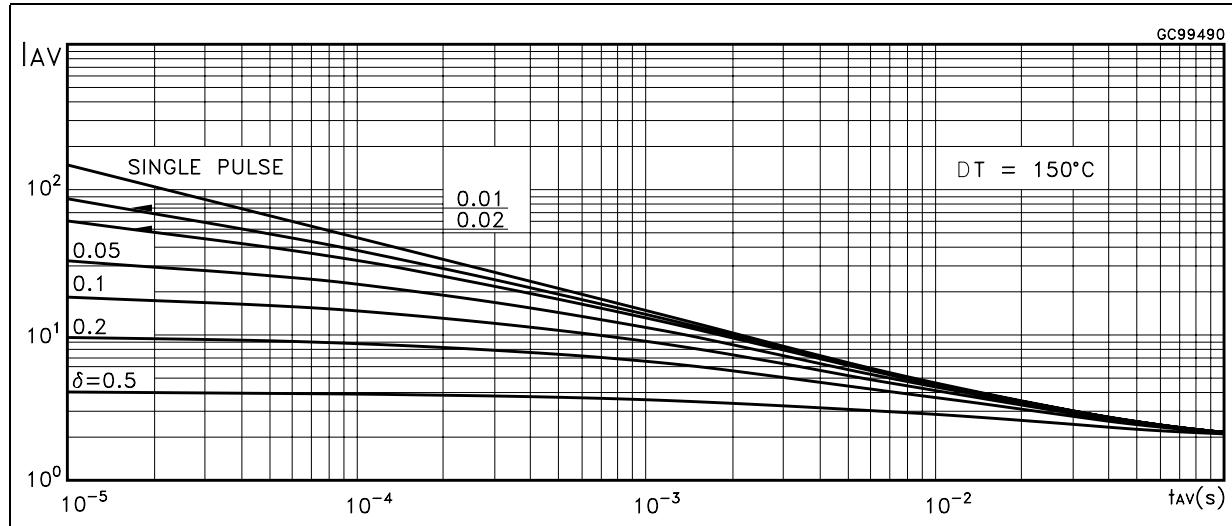
The previous curve gives the safe operating area for unclamped inductive loads, single pulse or repetitive, under the following conditions:

$$P_{D(AVE)} = 0.5 * (1.3 * B_{VDSS} * I_{AV})$$

$$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$$

Where:

I_{AV} is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

t_{AV} is the time in avalanche

To de rate above 25 °C, at fixed I_{AV}, the following equation must be applied:

$$I_{AV} = 2 * (T_{jmax} - T_{CASE}) / (1.3 * B_{VDSS} * Z_{th})$$

Where:

$Z_{th} = K * R_{th}$ is the value coming from normalized thermal response at fixed pulse width equal to T_{AV}.

3 Spice thermal model

Table 7. Spice parameter

Parameter	Node	Value
CTHERM1	7 - 6	$6 * 10^{-4}$
CTHERM2	6 - 5	$8 * 10^{-3}$
CTHERM3	5 - 4	$2 * 10^{-2}$
CTHERM4	4 - 3	$6 * 10^{-2}$
CTHERM5	3 - 2	$9.65 * 10^{-2}$
CTHERM6	2 - 1	$6 * 10^{-1}$
RTHERM1	7 - 6	0.045
RTHERM2	6 - 5	0.105
RTHERM3	5 - 4	0.150
RTHERM4	4 - 3	0.225
RTHERM5	3 - 2	0.375
RTHERM6	2 - 1	0.600

Figure 19. Thermal network
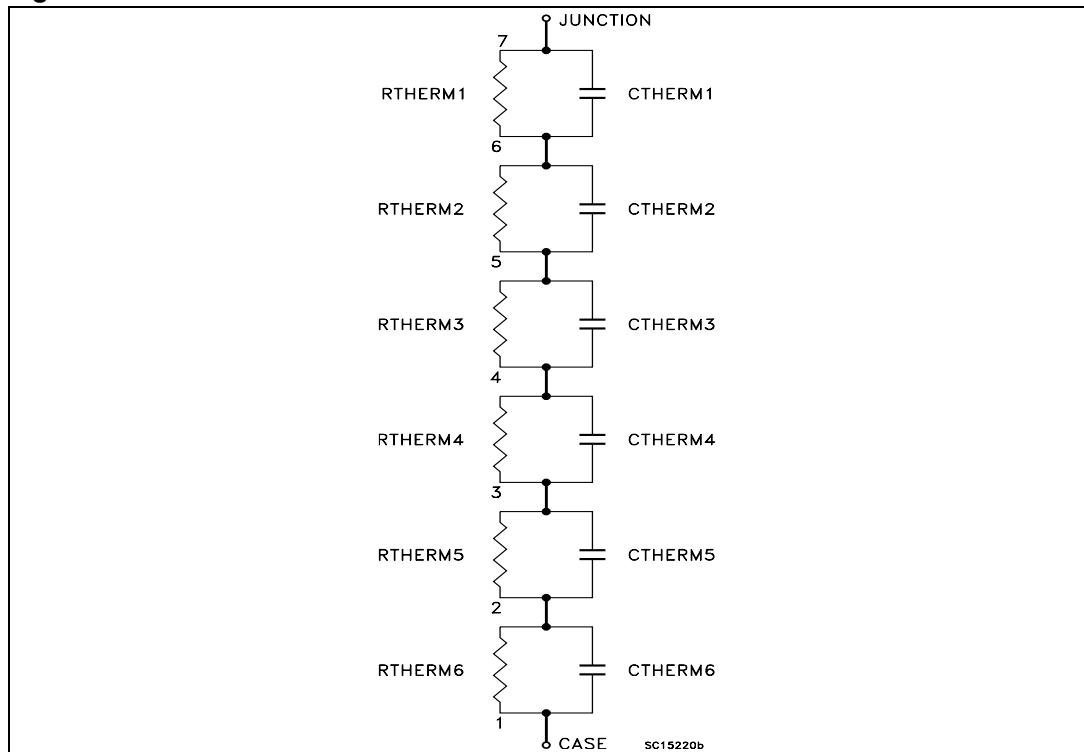
4   Test circuits

Figure 20.   Switching times test circuit for resistive load

AM01468v1
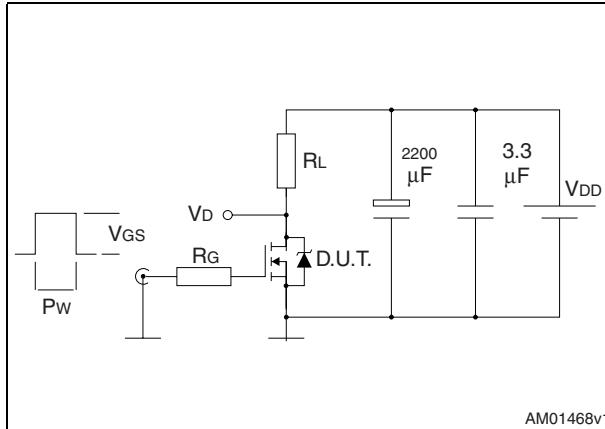
Figure 21.   Gate charge test circuit

AM01469v1
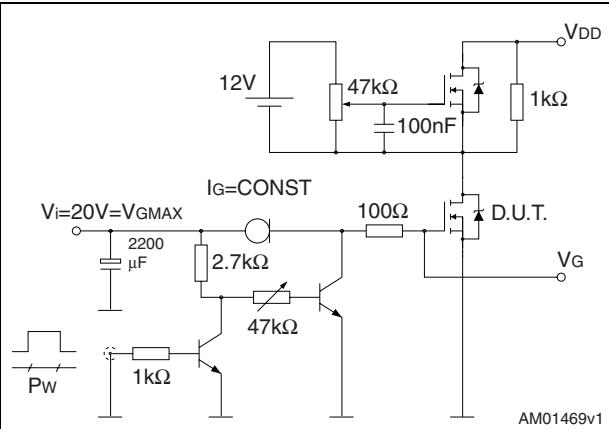
Figure 22.   Test circuit for inductive load switching and diode recovery times

AM01470v1
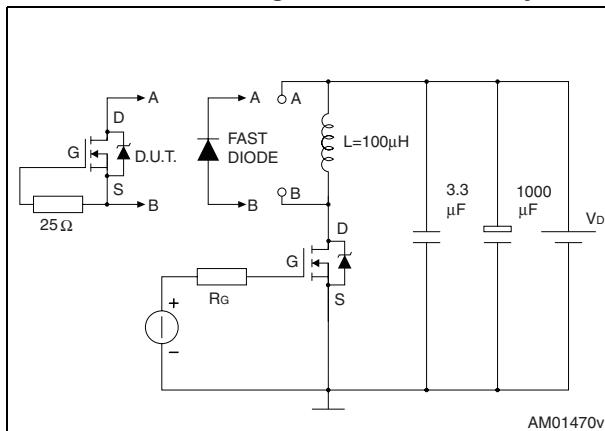
Figure 23.   Unclamped inductive load test circuit

AM01471v1
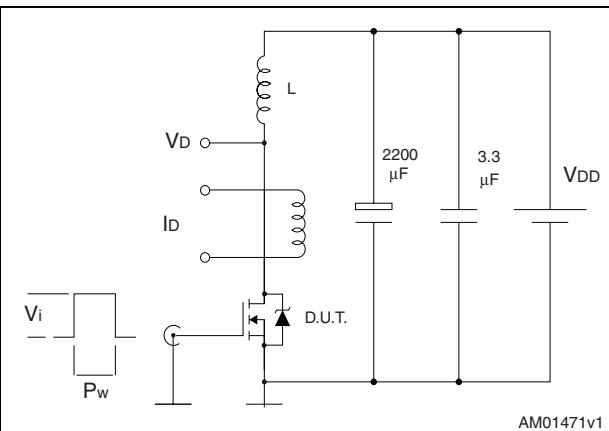
Figure 24.   Unclamped inductive waveform

AM01472v1
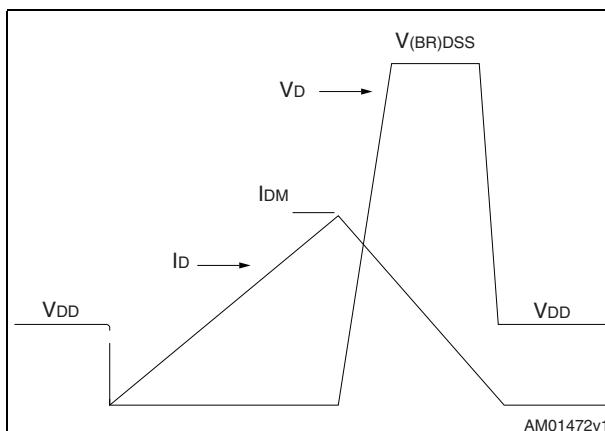
Figure 25.   Switching time waveform

AM01473v1
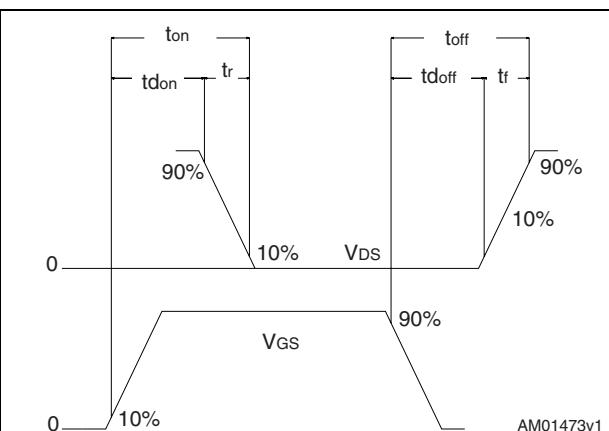
5 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °

TO-252 (DPAK) mechanical data

0068772_G
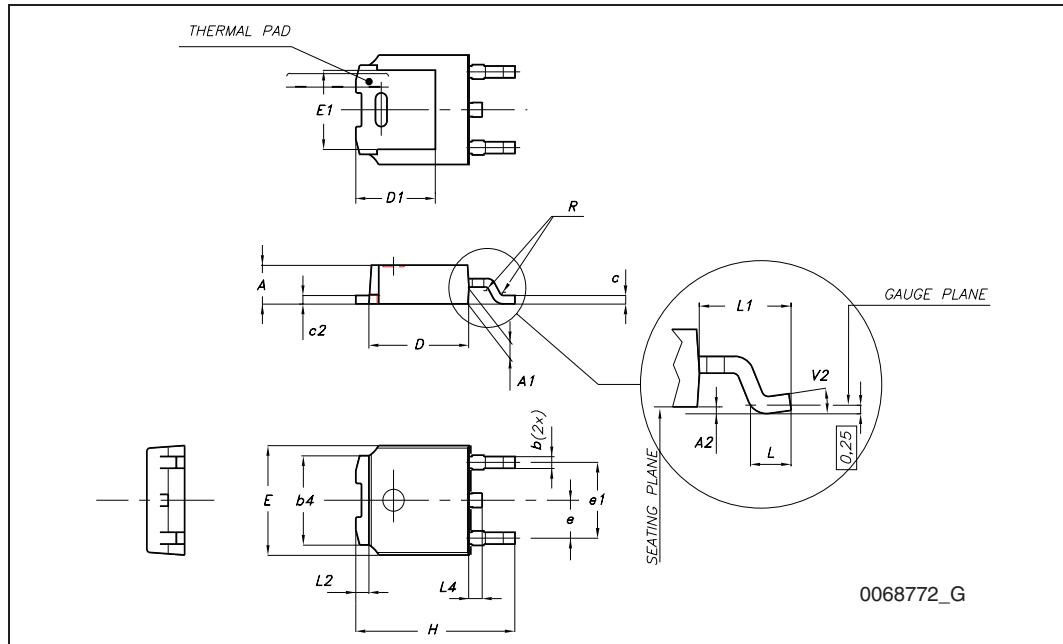
6 Packing mechanical data

DPAK FOOTPRINT

All dimensions are in millimeters

TAPE AND REEL SHIPMENT

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

7 Revision history

Table 8. Document revision history

Date	Revision	Changes
22-Jun-2004	1	Preliminary version
09-Sep-2004	2	Complete version
11-Jul-2006	3	New template, no content change
20-Feb-2007	4	Typo mistake on page 1
20-May-2009	5	*Figure 2* and *Figure 3* have been updated

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