

Description

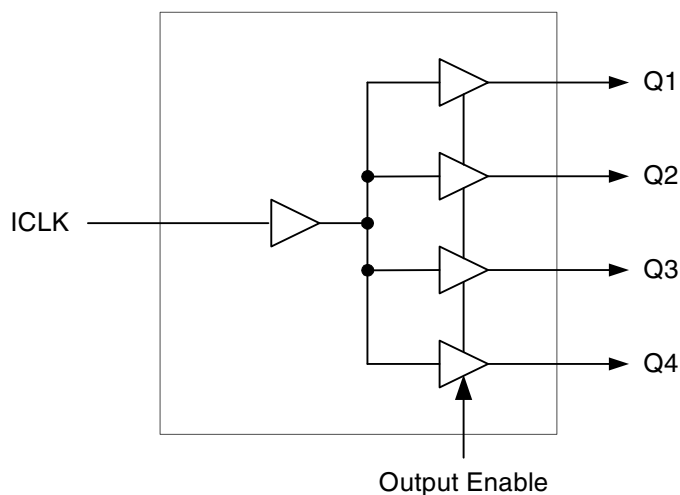
The 621S is a low cost, high-speed single input to four output clock buffer. The 621S has best in class Additive Phase Jitter of sub 50fsec.

IDT makes many non-PLL and PLL based low skew output devices as well as Zero Delay Buffers to synchronize clocks. Contact IDT for all of your clocking needs.

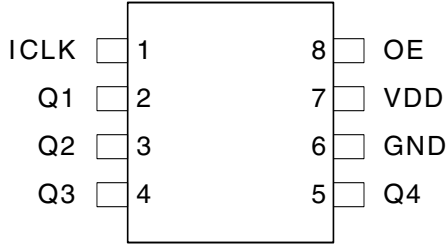
Features

- Low additive phase jitter RMS: 50fs
- Extremely low skew outputs (50ps)
- Low cost clock buffer
- Packaged in 8-pin SOIC and 8-pin DFN, Pb-free
- Input/Output clock frequency up to 200 MHz
- Non-inverting output clock
- Ideal for networking clocks
- Operating Voltages: 1.8V to 3.3V
- Output Enable mode tri-states outputs
- Advanced, low power CMOS process
- Extended temperature range (-40°C to +105°C)

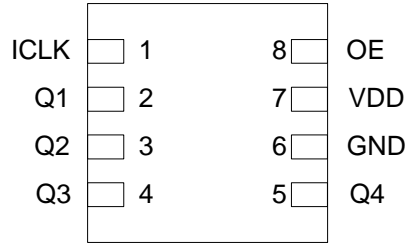
Block Diagram



Pin Assignment



8 Pin (150 mil) SOIC



8-pin DFN

Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description |
|------------|----------|----------|--|
| 1 | ICLK | Input | Clock input. Internal pull-up resistor. |
| 2 | Q1 | Output | Clock output 1. |
| 3 | Q2 | Output | Clock output 2. |
| 4 | Q3 | Output | Clock output 3. |
| 5 | Q4 | Output | Clock output 4. |
| 6 | GND | Power | Connect to ground. |
| 7 | VDD | Power | Connect +1.8V, +2.5V or +3.3V. |
| 8 | OE | Input | Output Enable. Tri-states outputs when low. Internal pull-up resistor. |

External Components

A minimum number of external components are required for proper operation. A decoupling capacitor of 0.01 μ F should be connected between VDD on pin 7 and GND on pin 6, as close to the device as possible. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 621S. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|------------------|
| Supply Voltage, VDD | 3.465V |
| All Inputs and Outputs | -0.5 V to 3.465V |
| Ambient Operating Temperature, Extended | -40 to +105°C |
| Storage Temperature | -65 to +150°C |
| Junction Temperature | 125°C |
| Soldering Temperature | 260°C |

Recommended Operation Conditions

| Parameter | Min. | Typ. | Max. | Units |
|---|-------|------|--------|-------|
| Ambient Operating Temperature, Extended | -40 | – | +105 | °C |
| Power Supply Voltage (measured in respect to GND) | +1.71 | | +3.465 | V |

DC Electrical Characteristics

VDD=1.8 V \pm 5%, Ambient temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|---------|------|---------|----------|
| Operating Voltage | VDD | | 1.71 | | 1.89 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | 0.7xVDD | | 1.89 | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Input High Voltage, OE | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -10 mA | 1.3 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 10 mA | | | 0.35 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 13 | | mA |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | OE pin | | 5 | | pF |

Notes: 1. Nominal switching threshold is VDD/2.

VDD=2.5 V \pm 5%, Ambient temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|---------|------|---------|----------|
| Operating Voltage | VDD | | 2.375 | | 2.625 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | 0.7xVDD | | 2.625 | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Input High Voltage, OE | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -16 mA | 1.8 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 16 mA | | | 0.5 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 18 | | mA |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | OE pin | | 5 | | pF |

Notes: 1. Nominal switching threshold is VDD/2.

VDD=3.3 V \pm 5%, Ambient temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--------------------------|-----------------|--------------------------|---------|------|---------|----------|
| Operating Voltage | VDD | | 3.135 | | 3.465 | V |
| Input High Voltage, ICLK | V _{IH} | Note 1 | 0.7xVDD | | 3.465 | V |
| Input Low Voltage, ICLK | V _{IL} | Note 1 | | | 0.3xVDD | V |
| Input High Voltage, OE | V _{IH} | | 0.7xVDD | | VDD | V |
| Input Low Voltage, OE | V _{IL} | | | | 0.3xVDD | V |
| Output High Voltage | V _{OH} | I _{OH} = -25 mA | 2.2 | | | V |
| Output Low Voltage | V _{OL} | I _{OL} = 25 mA | | | 0.7 | V |
| Operating Supply Current | IDD | No load, 135 MHz | | 22 | | mA |
| Nominal Output Impedance | Z _O | | | 17 | | Ω |
| Input Capacitance | C _{IN} | OE pin | | 5 | | pF |

Notes: 1. Nominal switching threshold is VDD/2.

AC Electrical Characteristics

VDD=1.8V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|--------|
| Output Frequency | | 5pF load, Note 4 | | | 200 | MHz |
| Output Clock Rise Time | t _{OR} | 0.36 to 1.44 V | | 0.6 | 1.0 | ns |
| Output Clock Fall Time | t _{OF} | 1.44 to 0.36V | | 0.6 | 1.0 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | | 135 MHz, Note 1 | 1.5 | 2 | 4 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration range: 12kHz–20MHz | | | 0.05 | ps |
| Output to Output Skew | | Rising edges at VDD/2, Note 2 | | 50 | 65 | ps |
| Output Enable Time | t _{EN} | CL ≤ 5pF | | | 3 | cycles |
| Output Disable Time | t _{DIS} | CL ≤ 5pF | | | 3 | cycles |

VDD=2.5V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|--------|
| Output Frequency | | 5pF load, Note 4 | | | 200 | MHz |
| Output Clock Rise Time | t _{OR} | 0.5 to 2.0V | | 0.6 | 1.0 | ns |
| Output Clock Fall Time | t _{OF} | 2.0 to 0.5V | | 0.6 | 1.0 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | | 135 MHz, Note 1 | 1.8 | 2.5 | 4.5 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration range: 12kHz–20MHz | | | 0.05 | ps |
| Output to Output Skew | | Rising edges at VDD/2, Note 2 | | 50 | 65 | ps |
| Output Enable Time | t _{EN} | CL ≤ 5pF | | | 3 | cycles |
| Output Disable Time | t _{DIS} | CL ≤ 5pF | | | 3 | cycles |

VDD=3.3 V ±5%, Ambient Temperature -40° to +105°C, unless stated otherwise

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------------|-----------------------|--|------|------|------|--------|
| Output Frequency | | 5pF load, Note 4 | | | 200 | MHz |
| Output Clock Rise Time | t _{OR} | 0.66 to 2.64V | | 0.6 | 1.0 | ns |
| Output Clock Fall Time | t _{OF} | 2.64 to 0.66V | | 0.6 | 1.0 | ns |
| Start-up Time | t _{START-UP} | Part start-up time for valid outputs after VDD ramp-up | | | 2 | ms |
| Propagation Delay | | 135 MHz, Note 1 | 1.5 | 2 | 4 | ns |
| Buffer Additive Phase Jitter, RMS | | 125MHz, Integration range: 12kHz–20MHz | | | 0.05 | ps |
| Output to Output Skew | | Rising edges at VDD/2, Note 2 | | 50 | 65 | ps |
| Output Enable Time | t _{EN} | CL ≤ 5pF | | | 3 | cycles |
| Output Disable Time | t _{DIS} | CL ≤ 5pF | | | 3 | cycles |

Notes:

1. With rail to rail input clock.
2. Between any 2 outputs with equal loading.
3. Duty cycle on outputs will match incoming clock duty cycle. Consult IDT for tight duty cycle clock generators.
4. With external series resistor of 33Ω positioned close to each output pin.

Phase Noise Plots

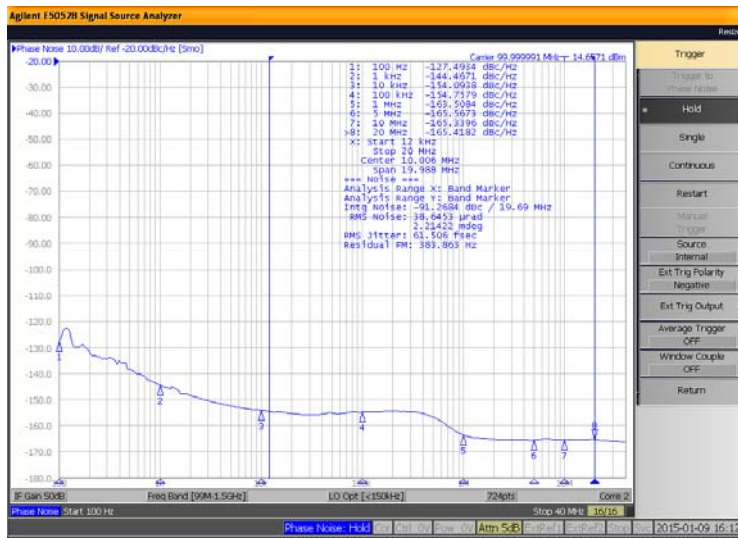


Figure 1. 621S Reference Phase Noise 62fs (12kHz to 20MHz)

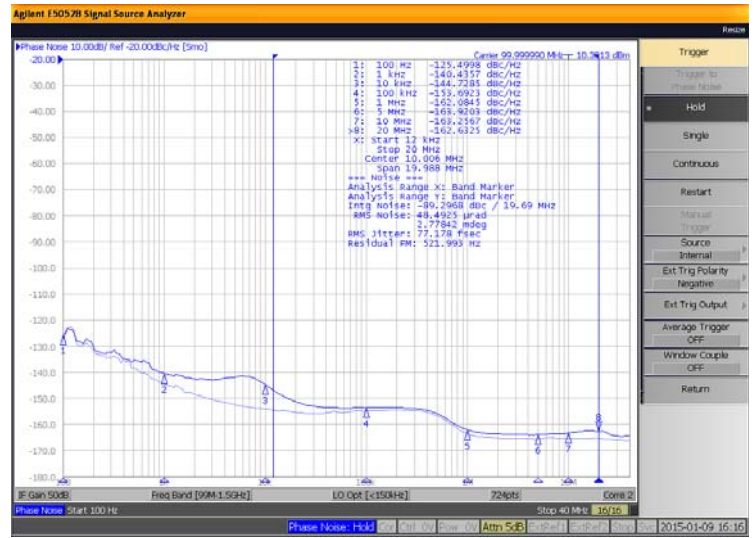
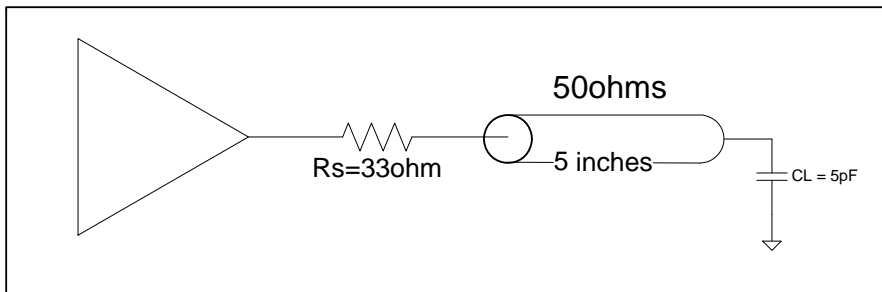


Figure 2. 621S Output Phase Noise 77fs (12kHz to 20MHz)

The phase noise plots above show the low Additive Jitter of the 621S high-performance buffer. With an integration range of 12kHz to 20MHz, the reference input has about 62fs of RMS phase jitter while the output of 621S has about 77fs of RMS phase jitter. This results in a low Additive Phase Jitter of only 45fs.

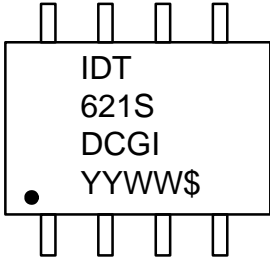
Test Load and Circuit



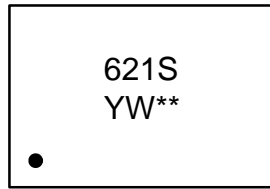
Thermal Characteristics (8SOIC)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 150 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 140 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 120 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 40 | | °C/W |

Marking Diagrams



8-pin SOIC

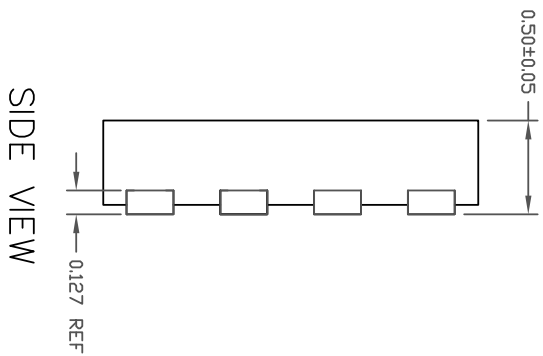
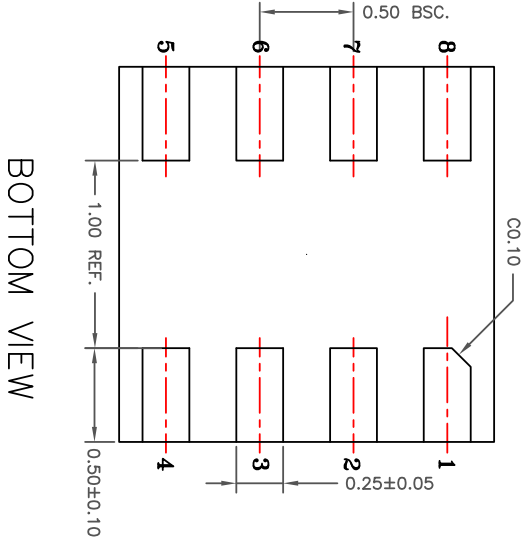
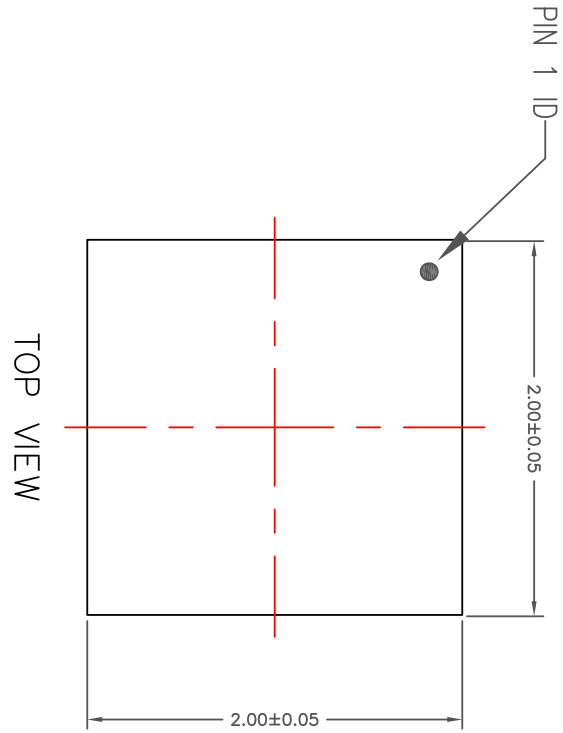


8-pin DFN

Notes:

1. “**” is the lot number.
2. “YYWW” or “YW” are the last digits of the year and week that the part was assembled.
3. “\$” denotes the mark code.
- 4 “G” denotes RoHS compliant package.
5. “I” denotes extended temperature range device.

Package Outline and Package Dimensions (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)

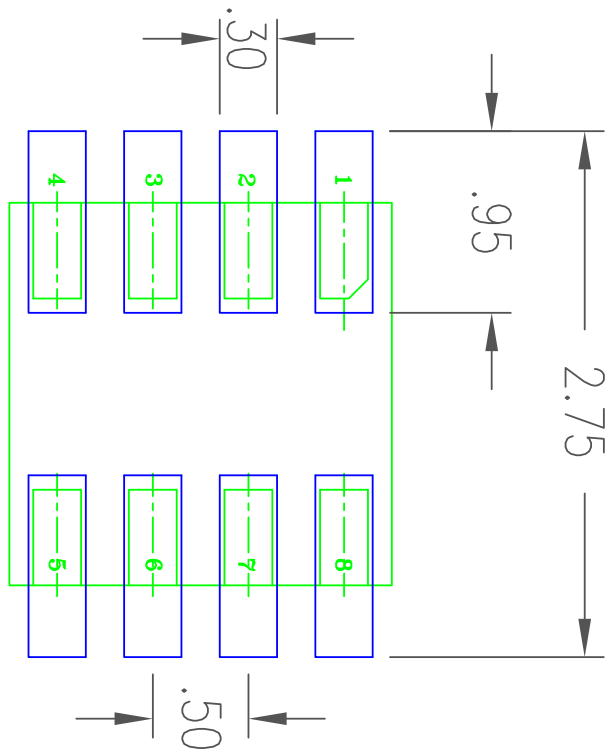


- NOTES:
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
 2. ALL DIMENSIONS ARE IN MILLIMETERS

| REVISIONS | | | |
|-----------|-----------------|----------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 09/18/14 | JHUA |

| | | | |
|---|----------|--|--------------|
| TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR ± XXXX XXXX | | IDT 6024 SILVER CREEK VALLEY ROAD San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 492-8674 | |
| APPROVALS | DATE | TITLE | SIZE |
| DRAWN 02/09/10/14 | 09/10/14 | 2.0 X 2.0 mm BODY | C |
| CHECKED 3/4/09/10/14 | 09/10/14 | 0.5mm PITCH VDFEN | DRAWING No. |
| | | | PSC-4490 |
| | | | REV 00 |
| DO NOT SCALE DRAWING | | | SHEET 1 OF 2 |

Package Outline and Package Dimensions, cont. (8-pin DFN, 2mm x 2mm Body, 0.5mm pitch)



RECOMMENDED LAND PATTERN DIMENSION

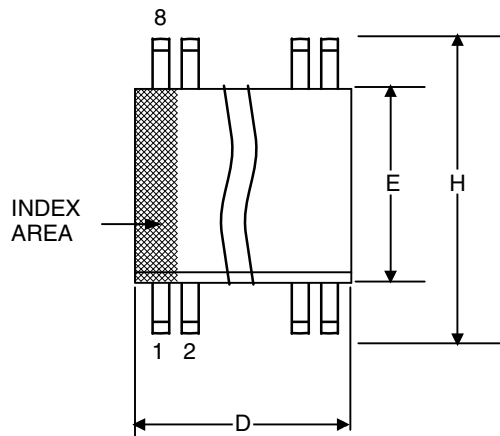
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR MOUNT DESIGN AND LAND PATTERN.

| REVISIONS | | |
|-----------|-----------------|--------|
| REV | DESCRIPTION | DATE |
| 00 | INITIAL RELEASE | 09/18/ |
| | | |
| | | |

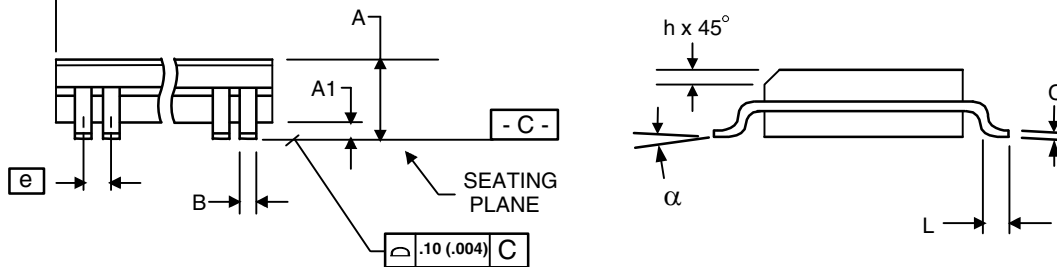
| | | | | | |
|-----------------------------|-------------|----------------------|-------------|---------|--|
| TOLERANCES UNLESS SPECIFIED | | DECIMAL | | ANGULAR | |
| XXX | ± | ° | | | |
| XXXX | ± | ° | | | |
| XXXXX | ± | ° | | | |
| APPROVALS | DATE | TITLE | | | |
| DRAWN | 02/09/10/14 | CMG8 PACKAGE OUTLINE | | | |
| CHECKED | | 2.0 X 2.0 mm BODY | | | |
| | | 0.5 mm PITCH VDFEN | | | |
| | | SIZE | DRAWING No. | | |
| | | C | PSC-4491 | | |
| | | DO NOT SCALE DRAWING | | | |

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Narrow Body)



| Symbol | Millimeters | | Inches* | |
|--------|-------------|------|-------------|-------|
| | Min | Max | Min | Max |
| A | 1.35 | 1.75 | .0532 | .0688 |
| A1 | 0.10 | 0.25 | .0040 | .0098 |
| B | 0.33 | 0.51 | .013 | .020 |
| C | 0.19 | 0.25 | .0075 | .0098 |
| D | 4.80 | 5.00 | .1890 | .1968 |
| E | 3.80 | 4.00 | .1497 | .1574 |
| e | 1.27 BASIC | | 0.050 BASIC | |
| H | 5.80 | 6.20 | .2284 | .2440 |
| h | 0.25 | 0.50 | .010 | .020 |
| L | 0.40 | 1.27 | .016 | .050 |
| a | 0° | 8° | 0° | 8° |

*For reference only. Controlling dimensions in mm.



Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|------------|--------------------|------------|----------------|
| 621SDCGI | see page 7 | Tubes | 8-pin SOIC | -40 to +105 °C |
| 621SDCGI8 | | Tape and Reel | 8-pin SOIC | -40 to +105 °C |
| 621SCMGI | | Cut Tape | 8-pin DFN | -40 to +105 °C |
| 621SCMGI8 | | Tape and Reel | 8-pin DFN | -40 to +105 °C |

“G” suffix to the part number denotes Pb-Free configuration, RoHS compliant.

Revision History

| Rev. | Date | Originator | Description of Change |
|------|---------|--------------|-----------------------|
| A | 03/1815 | B. Chandhoke | Initial release. |



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