MAXIM

CMOS 10-Bit A/D Converter with Track-and-Hold

MAX177

General Description

The MAX177 is a complete CMOS sampling 10-bit analog-to-digital converter (ADC) that combines an on-chip track-and-hold and voltage reference along with high conversion speed and low power consumption. A conversion time of 8.33µs includes settling time for the track-and-hold. An internal buried zener reference provides low drift with low noise.

The MAX177 accepts -2.5V to +2.5V inputs. External components are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry can either be driven from an external clock source or a crystal.

The MAX177 employs a standard microprocessor interface. Three-state data outputs can be configured for 8- or 12-bit data buses. Data access and bus release timing specs are compatible with most popular microprocessors without resorting to wait states.

Applications

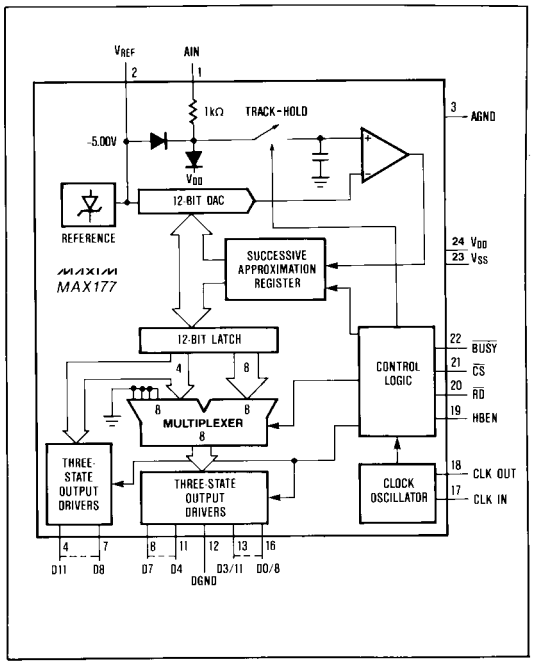
Digital Signal Processing (DSP)

Audio and Telecom Processing

High Accuracy Process Control

High Speed Data Acquisition

Functional Diagram



Features

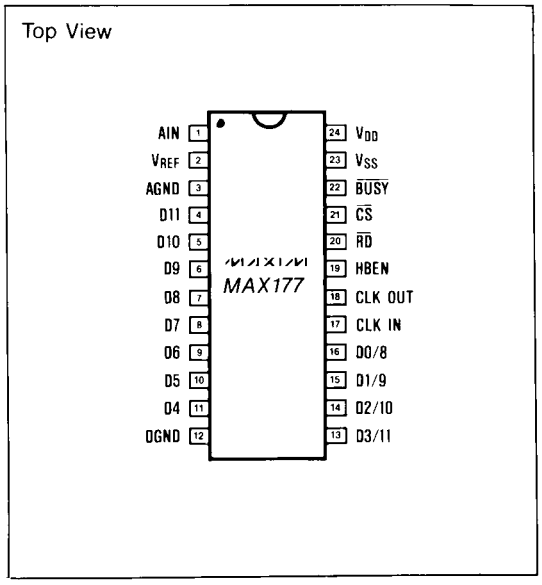
- ◆ **12-Bit Resolution and 10-Bit Linearity**
- ◆ **8.33µs Conversion Time**
- ◆ **Internal Analog Track-Hold**
- ◆ **6MHz Full Power Bandwidth**
- ◆ **On-Chip ±40ppm/°C Voltage Reference**
- ◆ **High Input Resistance (500MΩ)**
- ◆ **100ns Data Access Time**
- ◆ **180mW (Max) Power Consumption**
- ◆ **24 Lead Narrow DIP and Wide SO Packages**

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX177CNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX177CWG	0°C to +70°C	Wide SO	±1 LSB
MAX177C/D	0°C to +70°C	Dice**	±1 LSB
MAX177ENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX177EWG	-40°C to +85°C	Wide SO	±1 LSB
MAX177MRG	-55°C to +125°C	CERDIP	±1 LSB

* All devices — 24 lead packages
** Consult factory for dice specifications.

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V to V_{DD} +0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V to V_{DD} + 0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V to V_{DD} +0.3V
(Pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX177C ..... 0°C to +70°C
MAX177E ..... -40°C to +85°C
MAX177M ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode, T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.5MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Resolution			12			Bits
No Missing Code Resolution			10			Bits
Integral Non-Linearity	INL				0.05	%FSR
Offset Error (Note 1)					±8	mV
Full Scale Error (Note 2)		T_A = 25°C, Includes Reference Error			±0.4	%
Full Scale Tempco (Notes 3, 4)		Excludes Internal Reference Drift			±5	ppm/°C
Conversion Time	t_{CONV}	Synchronous (12.5 clock cycles) (13 clock cycles)			8.33 8.67	µs
DYNAMIC ACCURACY (V_{DD} = 5V, V_{SS} = 15V, Sample Rate = 100kHz)						
Signal to Noise and Distortion Ratio	S/(N+D)	10kHz Input Signal , T_A = 25°C	64			dB
Total Harmonic Distortion	THD	10kHz Input Signal, T_A = 25°C			-72	dB
Peak Harmonic or Spurious Noise		10kHz Input Signal, T_A = 25°C			-72	dB
Full Power Sampling Bandwidth		In Sample Mode, Under-Sampled Waveform		6		MHz
ANALOG INPUT						
Input Voltage Range			-2.5		+2.5	V
Input Leakage Current					±5	µA
Input Capacitance (Note 4)					20	pF
Track-Hold Acquisition Time			1			µs
REFERENCE						
V_{REF} Output Voltage		T_A = 25°C	-4.98	-5.00	-5.02	V
V_{REF} Output Tempco (Note 5)					±45	ppm/°C
Reference Load Sensitivity		$\Delta FS/\Delta I_{REF}$, I_{REF} Load Change: 0 to 5mA		0.005	0.02	%/mA
Output Sink Current					5	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode, T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.5MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN			0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN	2.4			V
Input Capacitance (Note 4)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN			10	pF
Input Current	I_{IN}	V_{IN} = 0V to V_{DD}; $\overline{CS}$, $\overline{RD}$, HBEN			10	µA
		CLK IN			20	
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLK OUT; I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLK OUT; I_{SOURCE} = 200µA	4			V
Three-State Leakage Current	I_L	D11-D0/8, V_{OUT} = 0V to V_{DD}			±10	µA
Three-State Output Capacitance (Note 4)	C_O				15	pF
POWER REQUIREMENTS						
Postive Supply Voltage	V_{DD}	±5% For Specified Performance		5		V
Negative Supply Voltage	V_{SS}	±5% For Specified Performance	-12		-15	V
Positive Supply Rejection		FS Change, V_{SS} = -15V or -12V; V_{DD} = 4.75 to 5.25V		±0.01		%
Negative Supply Rejection		FS Change, V_{DD} = 5V; V_{SS} = -14.24 to -15.75V; V_{SS} = -11.4 to -12.6V		±0.01		%
Positive Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		4	6	mA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		7	10	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -12V		104	150	mW

Note 1: Typical change over temp is ±1mV.
Note 2: Ideal last code transition = FS -1.8mV LSB, adjusted for offset.
Note 3: Full Scale Tempco = dFS/dT, where dFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: Guaranteed by design, not subject to test.
Note 5: V_{REF} Tempco = dV_{REF}//dT, where dV_{REF} is reference voltage change from T_A = 25°C to $T_{MIN}T_{MAX}$.
Note 6: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 7: This specification is 100% production tested.
Note 8: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 9: t_7 is defined as the time required for the data line to change 0.5V when loaded with the circuits of Figure 2.

For additional information on using the MAX177, please refer to MAX163/164/167data sheet.

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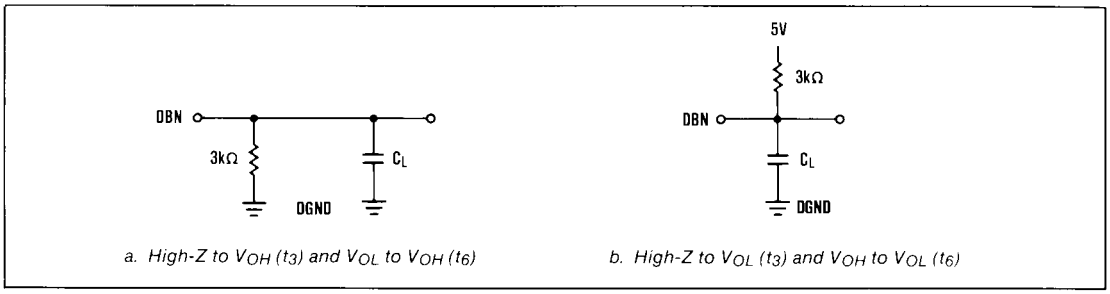
TIMING CHARACTERISTICS

(V_{DD} = +5V, V_{SS} = -12V or -15V, T_A = T_{MIN} to T_{MAX}, Note 6, specifications in bold type are 100% tested, others are guaranteed by design, unless otherwise noted.)

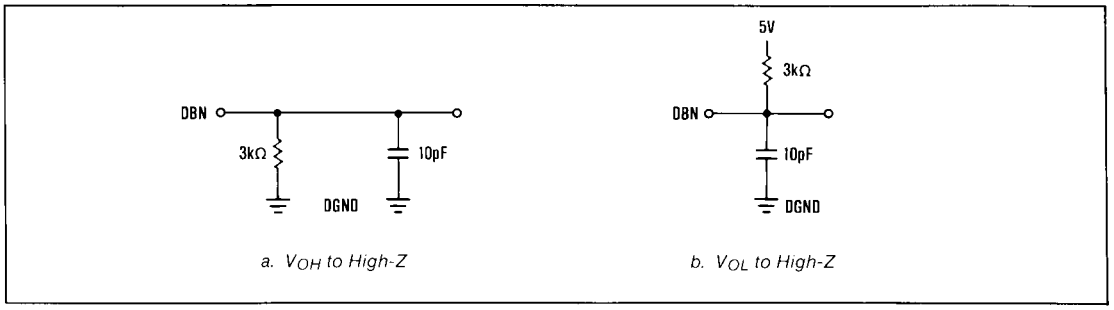
PARAMETER	SYMBOL	CONDITIONS	T_A = 25°C MIN	TYP	MAX	MAX177C/E MIN	MAX	MAX177M MIN	MAX	UNITS
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay (Note 7)	t_2	CL = 50pF		80	**170**		**220**		**260**	ns
Data Access Time (Notes 7, 8)	t_3	CL = 100pF		50	**100**		**130**		**150**	ns
$\overline{RD}$ Pulse Width	t_4		100			130		150		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ (Notes 7, 8)	t_6			40	**80**		**105**		**120**	ns
Bus Relinquish Time (Notes 7, 9)	t_7			30	**50**		**65**		**75**	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between READ Operations	t_{10}		200			200		200		ns
Delay Between Conversions	t_{11}		1			1		1		μs
Aperture Delay	t_{12}	Jitter < 50ps		25						ns



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Bus Relinquish Time