Features

- **Full Compliance with USB Spec Rev 1.1**
- **Four Downstream Ports**
- **Full-speed and Low-speed Data Transfers**
- **Bus-powered Controller**
- **Bus-powered or Self-powered Hub Operation**
- **Per Port Overcurrent Monitoring**
- **Individual Port Power Control**
- **USB Connection Status Indicators**
- **5V Operation with On-chip 3.3V Format**
- **32-lead SOIC and LQFP**

Self- and Bus-powered USB Hub Controller

AT43312A

Overview

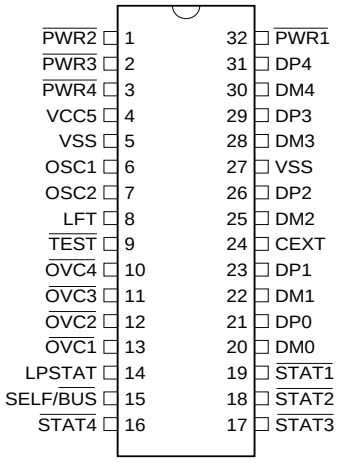
Introduction

The AT43312A is a 5 port USB hub chip supporting one upstream and four downstream ports. The AT43312A connects to an upstream hub or Host/Root Hub via Port0 and the other ports connect to external downstream USB devices. The hub re-transmits the USB differential signal between Port0 and Ports[1:4] in both directions. A USB hub with the AT43312A can operate as a bus-powered or self-powered through chip's power mode configuration pin. In the self-powered mode, port power can be switched or unswitched. Overcurrent reporting and port power control can be individual or global. An on-chip power supply eliminates the need for an external 3.3V supply.

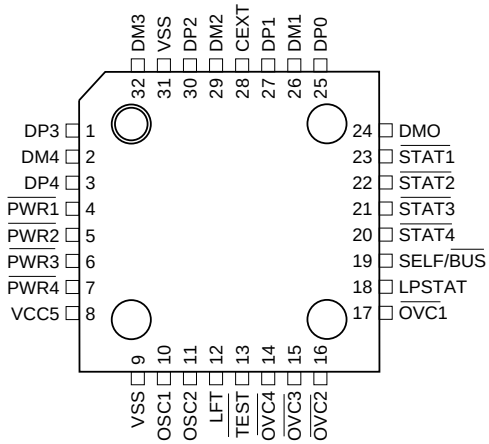
The AT43312A supports the 12-Mb/sec full speed as well as 1.5-Mb/sec slow speed USB transactions. To reduce EMI, the AT43312A's oscillator frequency is 6 MHz even though some internal circuitry operates at 48 MHz.

The AT43312A consists of a Serial Interface Engine, a Hub Repeater, and a Hub Controller.

SOIC



LQFP Top View



Rev. 1255F–USB–3/04

The Serial Interface Engine's Tasks are:

- Manage the USB communication protocol
- USB signaling detection/generation
- Clock/Data separation, data encoding/decoding, CRC generation/checking
- Data serialization/de-serialization

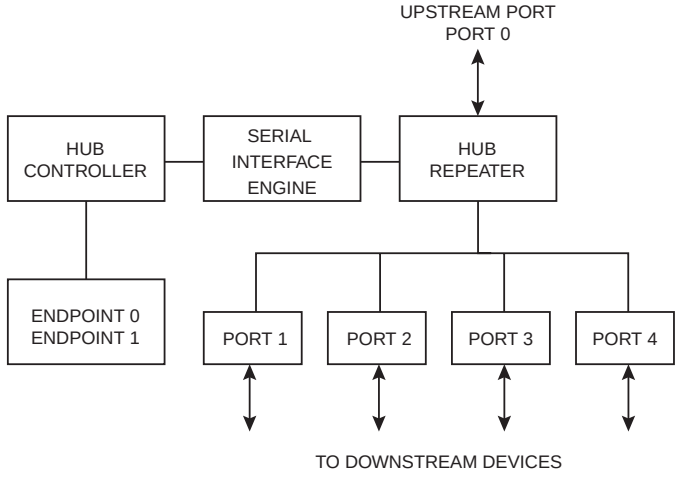
The Hub Repeater is Responsible for:

- Providing upstream connectivity between the selected device and the Host
- Managing connectivity setup and tear-down
- Handling bus fault detection and recovery
- Detecting connect/disconnect on each port

The Hub Controller is Responsible for:

- Hub enumeration
- Providing configuration information to the Host
- Providing status of each port to the Host
- Controlling each port per Host command

Figure 1. Block Diagram



Note: This document assumes that the reader is familiar with the Universal Serial Bus and therefore only describes the unique features of the AT43312A chip. For detailed information about the USB and its operation, the reader should refer to the Universal Serial Bus Specification Version 1.1, September 23, 1998.

Pin Assignment

Type: I = Input
O = Output
OD = Output, open drain
B = Bi-directional
V = Power supply, ground

Table 1. 32-lead SOIC Assignment

Pin	Signal	Type
1	$\overline{\text{PWR2}}$	O
2	$\overline{\text{PWR3}}$	O
3	$\overline{\text{PWR4}}$	O
4	VCC5	V
5	VSS	V
6	OSC1	I
7	OSC2	O
8	LFT	I
9	TEST	I
10	$\overline{\text{OVC4}}$	I
11	$\overline{\text{OVC3}}$	I
12	$\overline{\text{OVC2}}$	I
13	$\overline{\text{OVC1}}$	I
14	LPSTAT	I
15	SELF/$\overline{\text{BUS}}$	I
16	$\overline{\text{STAT4}}$	O

Pin	Signal	Type
17	$\overline{\text{STAT3}}$	O
18	$\overline{\text{STAT2}}$	O
19	$\overline{\text{STAT1}}$	O
20	DM0	B
21	DP0	B
22	DM1	B
23	DP1	B
24	CEXT	O
25	DM2	B
26	DP2	B
27	VSS	V
28	DM3	B
29	DP3	B
30	DM4	B
31	DP4	B
32	$\overline{\text{PWR1}}$	O

Table 2. 32-lead LQFP Assignment

Pin	Signal	Type
1	DP3	B
2	DM4	B
3	DP4	B
4	$\overline{\text{PWR1}}$	O
5	$\overline{\text{PWR2}}$	O
6	$\overline{\text{PWR3}}$	O
7	$\overline{\text{PWR4}}$	O
8	VCC5	V
9	VSS	V
10	OSC1	I
11	OSC2	O
12	LFT	I
13	$\overline{\text{TEST}}$	I
14	$\overline{\text{OVC4}}$	I
15	$\overline{\text{OVC3}}$	I
16	$\overline{\text{OVC2}}$	I

Pin	Signal	Type
17	$\overline{\text{OVC1}}$	I
18	LPSTAT	I
19	SELF/$\overline{\text{BUS}}$	I
20	$\overline{\text{STAT4}}$	O
21	$\overline{\text{STAT3}}$	O
22	$\overline{\text{STAT2}}$	O
23	$\overline{\text{STAT1}}$	O
24	DMO	B
25	DP0	B
26	DM1	B
27	DP1	B
28	CEXT	O
29	DM2	B
30	DP2	B
31	VSS	V
32	DM3	B

Signal Description

OSC1	Oscillator Input. Input to the inverting 6 MHz oscillator amplifier.
OSC2	Oscillator Output. Output of the inverting oscillator amplifier.
LFT	PLL Filter. For proper operation of the PLL, this pin should be connected through a 2.2 nF capacitor in parallel with a 100Ω resistor in series with a 10 nF capacitor to ground (VSS).
SELF/$\overline{\text{BUS}}$	Hub Power Mode. Input signal that sets the bus or self-powered mode operation. A high on this pin enables the self-powered mode, a low enables the bus-powered mode.
LPSTAT	Local Power Status. In the self-powered mode, this is an input pin that should be connected to the local power supply through a 47 kΩ resistor. The voltage on this pin is used by the chip for reporting the condition of the local power supply. In the bus-powered mode, this pin is not used.
DP0	Upstream Plus USB I/O. This pin should be connected to CEXT through an external 1.5 kΩ pull-up resistor. DP0 and DM0 form the differential signal pin pairs connected to the Host Controller or an upstream Hub.
DM0	Upstream Minus USB I/O.
DP[1:4]	Port Plus USB I/O. This pin should be connected to VSS through an external 15 kΩ resistor. DP[1:4] and DM[1:4] are the differential signal pin pairs to connect downstream USB devices.
DM[1:4]	Port Minus USB I/O. This pin should be connected to VSS through an external 15 kΩ resistor
$\overline{\text{OVC}}$[1:4]	Overcurrent. This is the input signal used to indicate to the AT43312A that an overcurrent is detected at the port. If $\overline{\text{OVCx}}$ is asserted, AT43312A will assert the $\overline{\text{PWRx}}$ pin and report the status to the USB Host.
$\overline{\text{PWR}}$[1:4]	Power Switch. This is an output signal used to enable or disable the external voltage regulator supplying power to a port. $\overline{\text{PWRx}}$ is de-asserted when a power supply problem is detected at $\overline{\text{OVCx}}$.
$\overline{\text{STAT}}$[1:4]	Connect Status. This is an output pin indicating that a port is properly connected. $\overline{\text{STATx}}$ is asserted when the port is enabled.
CEXT	External Capacitor. For proper operation of the on chip regulator, a 0.27 µF capacitor must be connected to this pin.
$\overline{\text{TEST}}$	Test. This pin should be connected to a logic high for normal operation.
VCC	5V Power Supply.
VSS	Ground.

Functional Description

Summary

The Atmel AT43312A is a USB hub controller for use in a standalone hub as well as an add-on hub for an existing non-USB peripheral such a PC display monitor or keyboard. In addition to supporting the standard USB hub functionality, the AT43312A has additional features to enhance the user friendliness of the hub.

USB Ports

The AT43312A's upstream port, Port0, is a full-speed port. A 1.5 kΩ pull-up resistor to the 3.3V regulator output, CEXT, is required for proper operation. The downstream ports support both full-speed as well as low-speed devices. 15 kΩ pull-down resistors are required at their inputs.

Full-speed signal requirements demand controlled rise/fall times and impedance matching of the USB ports. To meet these requirements, 22Ω resistors must be inserted in series between the USB data pins and the USB connectors.

Hub Repeater

The Hub Repeater is responsible for port connectivity setup and tear-down. It also supports exception handling such as bus fault detection and recovery, and connect/disconnect detection. Port0 is the root port and is connected to the root hub or an upstream hub. When a packet is received at Port0, the AT43312A propagates it to all the enabled downstream ports. Conversely, a packet from a downstream port is transmitted from Port0.

The AT43312A supports downstream port data signaling at both 1.5 Mb/s and 12 Mb/s. Devices attached to the downstream ports are determined to be either full-speed or low-speed depending which data line (DP or DM) is pulled high. If a port is enumerated as low-speed, its output buffers operate at a slew rate of 75 - 300 ns, and the AT43312A will not propagate any traffic to that port unless it is prefaced with a preamble PID. Low-speed data following the preamble PID is propagated to both low- and full-speed devices. The AT43312A will enable low-speed drivers within four full-speed bit times of the last bit of a preamble PID, and will disable them at the end of an EOP. Packets out of Port0 are always transmitted using the full-speed drivers.

All the AT43312A ports independently drive and monitor their DP and DM pins so that they are able to detect and generate the "J", "K", and SE0 bus signaling states. Each hub port has single-ended and differential receivers on its DP and DM lines. The port I/O buffers comply with the voltage levels and drive requirements as specified in the USB Specifications Rev 1.0.

The Hub Repeater implements a frame timer which is timed by the 12 MHz USB clock and gets reset every time an SOF token is received from the Host.

Serial Interface Engine

The Serial Interface Engine handles the USB communication protocol. It performs the USB clock/data separation, the NRZI data encoding/decoding, bit stuffing, CRC generation and checking, USB packet ID decoding and generation, and data serialization and de-serialization. The on chip phase locked loop generates the high frequency clock for the clock/data separation circuit.

Power Management

A hub is a high-powered device and is allowed to draw up to 500 mA of current from the host or upstream hub. The AT43312A chip itself and its external hub circuitry consume much less than 100 mA. The AT43312A's power management logic works with external devices to detect overcurrent and control power to the ports.

Overcurrent sensing is on a per-port basis and is achieved through the $\overline{OVCx}$ pins. Whenever the voltage at $\overline{OVCx}$ is asserted, the AT43312A treats it as an overcurrent condition. This could be caused by an overload, or even a short circuit and could cause the AT43312A to set the port's PORT_OVER_CURRENT status bit and its C_PORT_OVER_CURRENT status change bit. At the same time, power to the offending port is shut off and its $\overline{STATx}$ generates a square wave with a frequency of about 1 second.

An external device is needed to monitor the overcurrent condition and perform the actual switching of the ports' power under control of the AT43312A. Any type of suitable switch or device is acceptable. However, it should have a low-voltage drop across it even when the port absorbs full-power. In its simplest form this switch can be a P-channel MOSFET. One advantage of using a MOSFET switch is its very low-voltage drop and low-cost.

Each one of the AT43312A's port has its own power control pin which is asserted only when a SetPortFeature[PORT-POWER] request is received from the host. $\overline{PWRx}$ is de-asserted under the following conditions:

1. Power-up
2. Reset and initialization
3. Overcurrent condition
4. Requested by the host through a ClearPortFeature [PORT_POWER] for ALL the ports

Self-powered Mode

In the self-powered mode, power to the downstream ports must be supplied by an external power supply. This power supply must be capable of supplying 500 mA per port for a total of 2A.

The USB specifications require that the voltage drop at the power switch and board traces be no more than 100 mV. A good conservative maximum drop at the power switch itself should be no more than 75 mV. Careful design and selection of the power switch and PC board layout is required to meet the specifications. When using a MOSFET switch, its resistance must be 140 mΩ or less under worst case conditions. A suitable MOSFET switch for an AT43312A based hub is an integrated high side dual MOSFET switch such as the Micrel MIC2526.

Bus Powered Mode

In the bus powered mode, all the power for the hub itself as well as the downstream ports is supplied by the root hub or upstream hub through the USB. Only 100 mA is available for each of the hub's downstream devices and therefore only low power devices are supported.

The power switch and overcurrent protection works exactly like the self-powered mode, except that the allowable switch resistance is higher: 700 mΩ or less under the worst case condition.

The diagrams of Figure 2 and Figure 3 show examples of the power supply and management connections for a typical AT43312A port in the self-powered mode and bus powered mode.

Figure 2. Self-powered Hub Power Supply

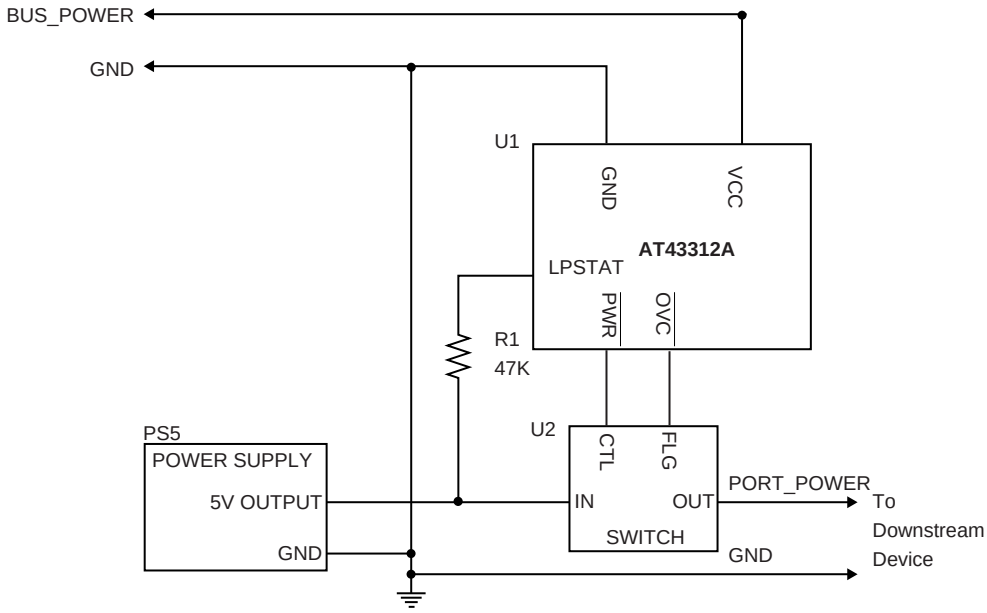
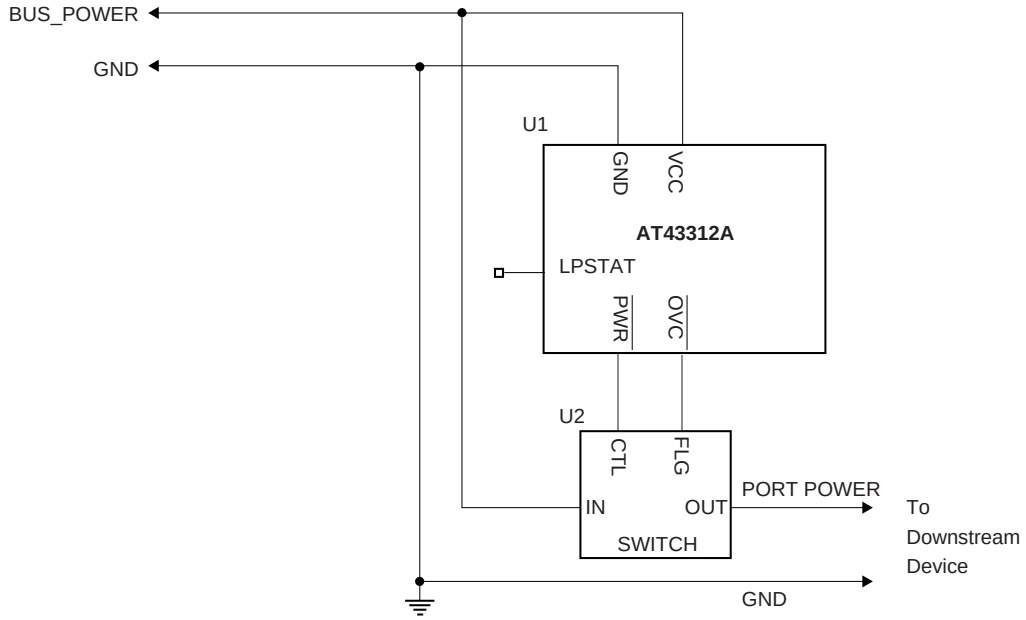


Figure 3. Bus Powered Hub Power Supply



Port Status Pin

The $\overline{\text{STATx}}$ pins are signals that is not required by the USB specification. Its function is to allow the hub to provide feedback to the user whenever a device is properly connected to the port. An LED and series resistor connected to $\overline{\text{STATx}}$ can be used to provide a visual feedback. If an overcurrent condition is detected at a port, the $\overline{\text{STATx}}$ of the offending port will alternately turn on and off causing an LED to blink. The LED will continue to blink until power to the offending port is turned off by the host or until the hub is re-enumerated.

The default state of $\overline{\text{STATx}}$ is inactive. After a port is enabled AT43312A will assert the port's $\overline{\text{STATx}}$. Any condition that causes the port to be disabled inactivates $\overline{\text{STATx}}$.

Note: The I/O Pins of the AT43312A should not be directly connected to voltages less than VSS or more than the voltage at the CEXT pins. If it is necessary to violate this rule, insert a series resistor between the I/O pin and the source of the external signal source that limits the current into the I/O pin to less than 2 mA. Under no circumstances should the external voltage exceed 5.5V. To do so will put the chip under excessive stress.

Hub Controller

The Hub Controller of the AT43312A provides the mechanism for the Host to enumerate the Hub and the AT43312A to provide the Host with its configuration information. It also provides a mechanism for the Host to monitor and control the downstream ports. Power is applied, on a per port basis, by the Hub Controller upon receiving a command, SetPortFeature[PORT_POWER], from the Host. The AT43312A must be configured first by the Host before the Hub Controller can apply power to external devices.

The Hub Controller contains two endpoints, Endpoint0 and Endpoint1 and maintains a status register, Controller Status Register, which reflects the AT43312A's current settings. At power up, all bits in this register will be set to 0's.

Table 3. Control Status Register

Bit	Function	Value	Description
0	Hub configuration status	0 1	Set to 0 or 1 by a Set_Configuration Request Hub is not currently configured Hub is currently configured
1	Hub remote wakeup status	0 1	Set to 0 or 1 by ClearFeature or SetFeature request Default value is 0 Hub is currently not enabled to request remote wakeup Hub is currently enabled to request remote wakeup
2	Endpoint0 STALL status	0 1	Endpoint0 is not stalled Endpoint0 is stalled
3	Endpoint1 STALL status	0 1	Endpoint1 is not stalled Endpoint1 is stalled

Endpoint 0

Endpoint 0 is the AT43312A's default endpoint used for enumeration of the Hub and exchange of configuration information and requests between the Host and the AT43312A. Endpoint 0 supports control transfers.

The Hub Controller supports the following descriptors: Device Descriptor, Configuration Descriptor, Interface Descriptor, Endpoint Descriptor, and Hub Descriptor. These Descriptors are described in detail elsewhere in this document. Standard USB Device Requests and class-specific Hub Requests are also supported through Endpoint 0. There is no endpoint descriptor for Endpoint0.

Endpoint 1

Endpoint1, an interrupt endpoint, is used by the Hub Controller to send status change information to the Host. The Hub Controller samples the changes at the end of every frame at time marker EOF2 in preparation for a potential data transfer in the subsequent frame. The sampled information is stored in a byte wide register, the Status Change Register, using a bitmap scheme.

Each bit in the Status Change Register corresponds to one port as shown on the following page.

Table 4. Status Change Register

Bit	Function	Value	Meaning
0	Hub status change	0 1	No change in status Change in status detected
1	Port1 status change	0 1	No change in status Change in status detected
2	Port2 status change	0 1	No change in status Change in status detected
3	Port3 status change	0 1	No change in status Change in status detected
4	Port4 status change	0 1	No change in status Change in status detected
5-7	Reserved	000	Default values

An IN Token packet from the Host to Endpoint 1 indicates a request for port change status. If the Hub has not detected any change on its ports, or any changes in itself, then all bits in this register will be 0 and the Hub Controller will return a NAK to requests on Endpoint1. If any of bits 0 - 4 is 1, the Hub Controller will transfer the whole byte. The Hub Controller will continue to report a status change when polled until that particular change has been removed by a ClearPortFeature request from the Host. No status change will be reported by Endpoint 1 until the AT43312A has been enumerated and configured by the Host via Endpoint 0.

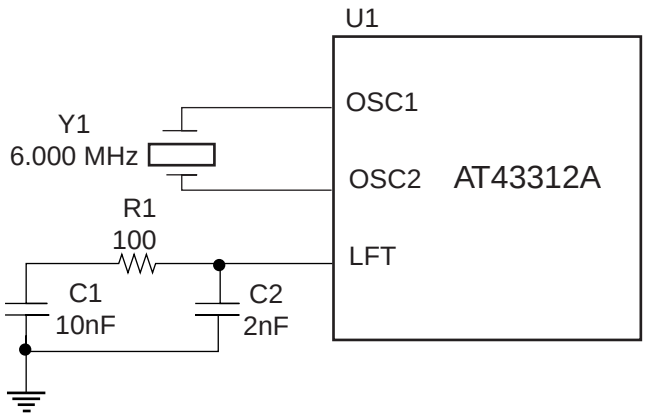
Oscillator and Phase-Locked-Loop

All the clock signals required to run the AT43311 are derived from an on-chip oscillator. To reduce EMI and power dissipation in the system, the oscillator is designed to operate with a 6 MHz crystal. An on-chip PLL generates the high frequency for the clock/data separator of the Serial Interface Engine. In the suspended state, the oscillator circuitry is turned off. To assure quick startup, a crystal with a high Q, or low ESR, should be used. To meet the USB hub frequency accuracy and stability requirements for hubs, the crystal should have an accuracy and stability of better than 100 PPM. Even though the oscillator circuit would work with a ceramic resonator, its use is not recommended because a resonator would not have the frequency accuracy and stability.

A 6 MHz parallel resonance quartz crystal with a load capacitance of approximately 10 pF is recommended. The oscillator is a special low-power design and in most cases no external capacitors and resistors are necessary. If the crystal requires a higher value capacitance, external capacitors can be added to the two terminals of the crystal and ground to meet the required value. If the crystal used cannot tolerate the drive levels of the oscillator, a series resistor between OSC2 and the crystal pin is recommended.

The clock can also be externally sourced. In this case, connect the clock source to the OSC1 pin, while leaving OSC2 pin floating. The switching level at the OSC1 pin can be as low as 0.47V (see Table 8) and a CMOS device is required to drive this pin to maintain good noise margins at the low switching level.

Figure 4. Oscillator and PLL Connections



For proper operation of the PLL, an external RC filter consisting of a series RC network of 100Ω and 10 nF in parallel with a 2 nF capacitor must be connected from the LFT pin to VSS.

To provide the best operating condition for the AT43312A, careful consideration of the power supply connections are recommended. Use short, low-impedance connections to all power supply lines: VCC5, and VSS. Use sufficient decoupling capacitors to reduce noise: 0.1 µF decoupling capacitors of high quality, soldered as close as possible to the package pins are recommended.

Power Supply

The AT43312A is powered from the USB bus, but has an internal voltage regulator to supply the 3.3V operating power to its circuitry. For proper operation, an external high quality, low ESR, 0.27 µF or larger, capacitor should be connected to the output of the regulator, CEXT pin and ground. The CEXT pin can also be used to supply the voltage to the 1.5K pull-up resistor at Port 0's DP pin.

To provide the best operating condition for the AT43312A, careful consideration of the power supply connections are recommended. Use short, low impedance connections to both power supply lines: VCC and VSS. Use sufficient decoupling capacitance to reduce noise: 0.1 µF of high quality ceramic capacitor soldered as close as possible to the VCC and VSS package pins. Package pins are recommended.

The AT43312A can also operate directly off a 3.3V power supply. In this case, leave the VCC pin floating and connect the 3.3V power to the CEXT pin.

Electrical Specification

Absolute Maximum Ratings*

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC5}	5V Power Supply			5.5	V
V_I	DC Input Voltage		-0.3V	V_{CEXT} + 0.3 4.6 max	V
V_O	DC Output Voltage		-0.3	V_{CEXT} + 0.3 4.6 max	V
T_O	Operating Temperature		-40	+125	°C
T_S	Storage Temperature		-65	+150	°C

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

The values shown in this table are valid for T_A = 0°C to 85°C, V_{CC} = 4.4 to 5.25V, unless otherwise noted.

Table 5. Power Supply

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	5V Power Supply		4.4	5.25	V
I_{CC}	5V Supply Current			24	mA
I_{CCS}	Suspended Device Current			150	µA

Table 6. USB Signals: DPx, DMx

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input Level High (driven)		2.0		V
V_{IHZ}	Input Level High (floating)		2.7		V
V_{IL}	Input Level Low			0.8	V
V_{DI}	Differential Input Sensitivity	DPx and DMx	0.2		V
V_{CM}	Differential Command Mode Range		0.8	2.5	V
V_{OL1}	Static Output Low	RL of 1.5 kΩ to 3.6V		0.3	V
V_{OH1}	Static Output High	RL of 1.5 kΩ to GND	2.8	3.6	V
V_{CRS}	Output Signal Crossover		1.3	2.0	V
C_{IN}	Input Capacitance			20	pF

Table 7. $\overline{PWR}$, $\overline{STAT}$, $\overline{OVC}$

Symbol	Parameter	Condition	Min	Max	Unit
V_{OL2}	Output Low Level, $\overline{PWR}$, $\overline{STAT}$, OVC	I_{OL} = 4 mA		0.5	V
V_{OH2}	Output High Level, $\overline{PWR}$	I_{OH} = 4 mA	0.5 V_{CEXT}		V
C_{out}	Output Capacitance	1 MHz		10	pF
V_{IL3}	Input Low Level			0.3 V_{CEXT}	V
V_{IH3}	Input High Level		0.7 V_{CEXT}		V
C_{out}	Output Capacitance	1 MHz		10	pF

Table 8. Oscillator Signals: OSC1, OSC2

Symbol	Parameter	Condition	Min	Max	Unit
V_{LH}	OSC1 Switching Level		0.47	1.20	V
V_{HL}	OSC1 Switching Level		0.67	1.44	V
C_{X1}	Input Capacitance, OSC1			17	pF
C_{X2}	Output Capacitance, OSC2			17	pF
C_{12}	Osc1/2 Capacitance			1	pF
t_{su}	Start-up Time	6 MHz, fundamental		2	ms
D_L	Drive Level	V_{CC} = 3.3V, 6 MHz crystal, 100Ω equiv. series resistor		150	µW

Note: OSC2 must not be used to drive other circuitry.

Table 9. DPx, DMx Driver Characteristics, Full-speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise Time	C_L = 50 pF	4	20	ns
t_F	Fall Time	C_L = 50 pF	4	20	ns
t_{RFM}	TR/TF Matching		90	110	%
z_{DRV}	Driver Output Resistance(Note:)	Steady state drive	28	44	Ω

Note: With external 22Ω series resistor.

Figure 5. Data Signal Rise and Fall Time

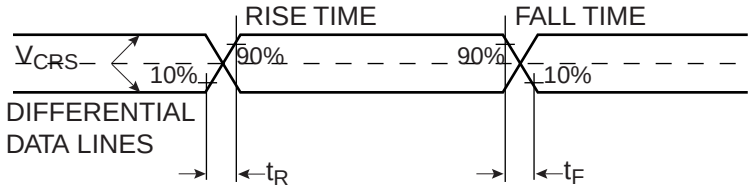


Table 10. DPx, DMx Source Timings, Full-speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_{DRATEq}	Full Speed Data Rate(1)	Average Bit Rate	11.97	12.03	Mb/s
t_{FRAME}	Frame Interval(1)		0.9995	1.0005	ms
t_{RFI}	Consecutive Frame Interval Jitter(1)	No clock adjustment		42	ns
t_{RFIADJ}	Consecutive Frame Interval Jitter(1)	No clock adjustment		126	ns
	Source Diff Driver Jitter				
t_{DJ1}	To Next Transition		-2	2	ns
t_{DJ2}	For Paired Transitions		-1	1	ns
t_{FDEOP}	Source Jitter for Differential Transition to SEO Transitions		-2	5	ns
t_{DEOP}	Differential to EOP Transition Skew		-2	5	ns
	Recvr Data Jitter Tolerance				
t_{JR1}	To Next Transition		-18.5	18.5	ns
t_{JR2}	To Paired Transitions		-9	9	ns
t_{FEOPT}	Source SEO Interval of EOP		160	175	ns
t_{FEOPR}	Receiver SEO Interval of EOP		82		ns
t_{FST}	Width of SEO Interval During Differential Transition			14	ns

Note: 1. With 6.000 MHz, 100 ppm crystal.

Figure 6. Full-speed Load

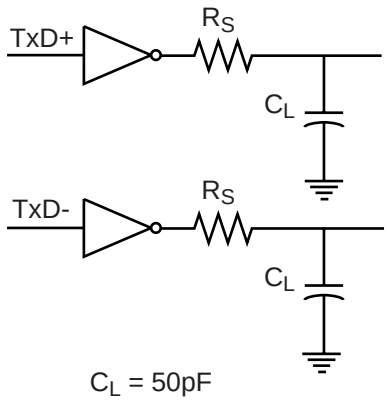
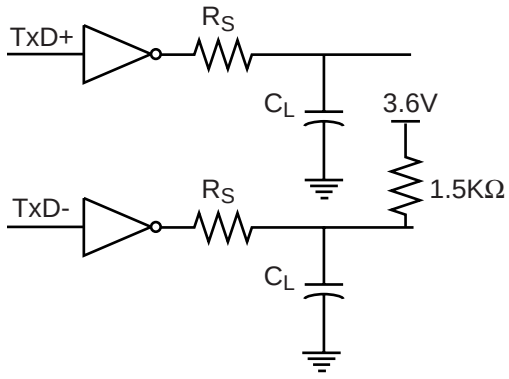


Table 11. DPx, DMx Driver Characteristics, Low-speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_R	Rise Time	CL = 200 - 600 pF	75	300	ns
t_F	Fall Time	CL = 200 - 600 pF	75	300	ns
t_{RFM}	TR/TF Matching		80	125	%

Figure 7. Low-speed Downstream Port Load



C_L = 200pF to 600pF

Table 12. DPx, DMx Hub Timings, Full-speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_{HDD2}	Hub Differential Data Delay without Cable			44	ns
	Hub Diff Driver Jitter				
t_{HDJ1}	To Next Transition		-3	3	ns
t_{HDJ2}	To Paired Transition		-1	1	ns
t_{FSOP}	Data Bit Width Distortion after SOP		-5	5	ns
t_{FEOPD}	Hub EOP Delay Relative to THDD		0	15	ns
t_{FHESK}	Hub EOP Output Width Skew		-15	15	ns

Table 13. DPx, DMx Hub Timings, Low-speed Operation

Symbol	Parameter	Condition	Min	Max	Unit
t_{LHDD}	Hub Differential Data Delay			300	ns
	Downstr Hub Diff Driver Jitter				
t_{LHDJ1}	To Next Transition, downst		-45	45	ns
t_{LHDJ2}	For Paired Transition, downst		-15	15	ns
t_{LUKJ1}	To Next Transition, upstr		-45	45	ns
t_{LUKJ2}	For Paired Transition, upstr		-45	45	ns
t_{SOP}	Data Bit Width Distortion after SOP		-60	60	ns
t_{LEOPD}	Hub EOP Delay Relative to THDD		0	200	ns
t_{LHESK}	Hub EOP Output Width Skew		-300	300	ns

Figure 8. Differential Data Jitter

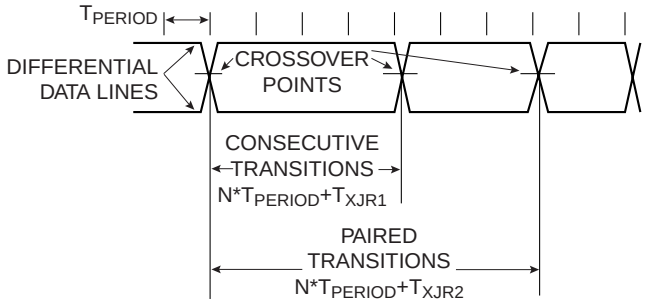


Figure 9. Differential-to-EOP Transition Skew and EOP Width

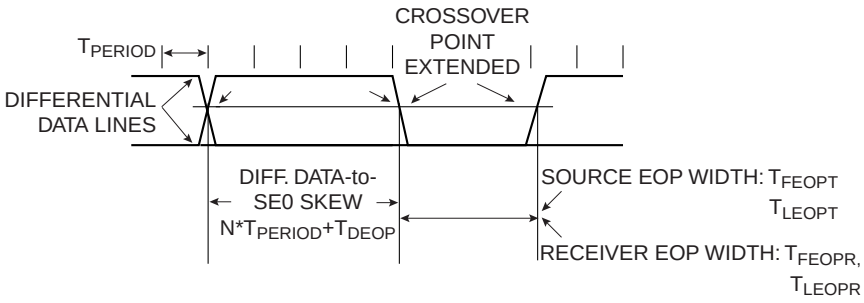


Figure 10. Receiver Jitter Tolerance

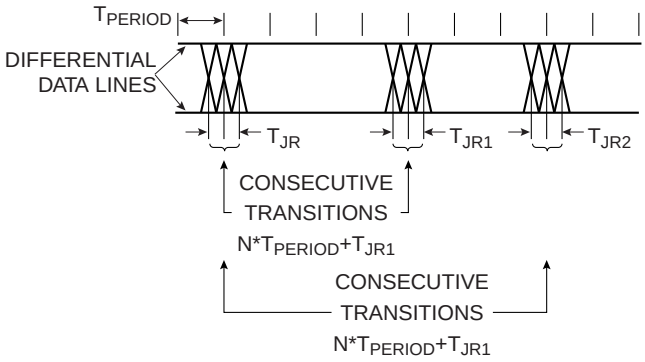


Figure 11. Hub Differential Delay, Differential Jitter, and SOP Distortion

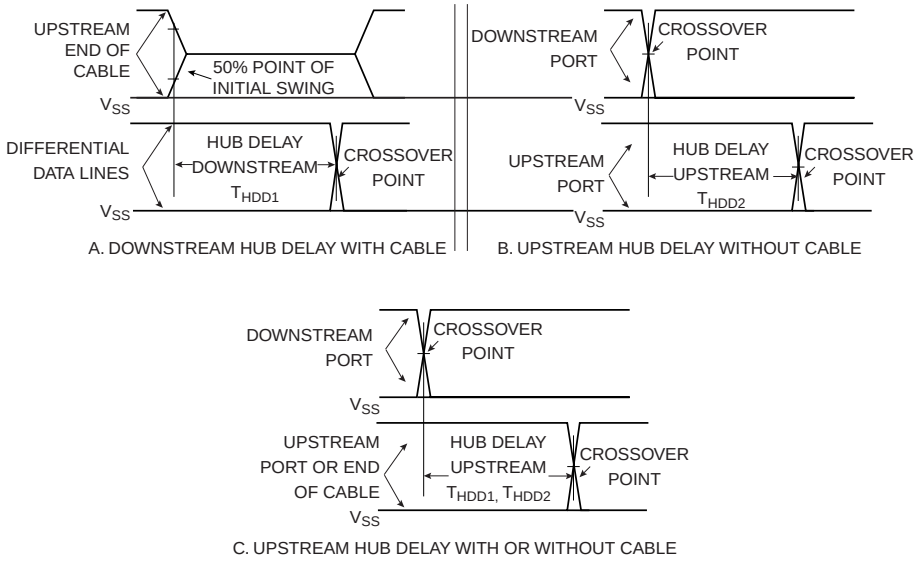


Figure 12. Hub EOP Delay and EOP Skew

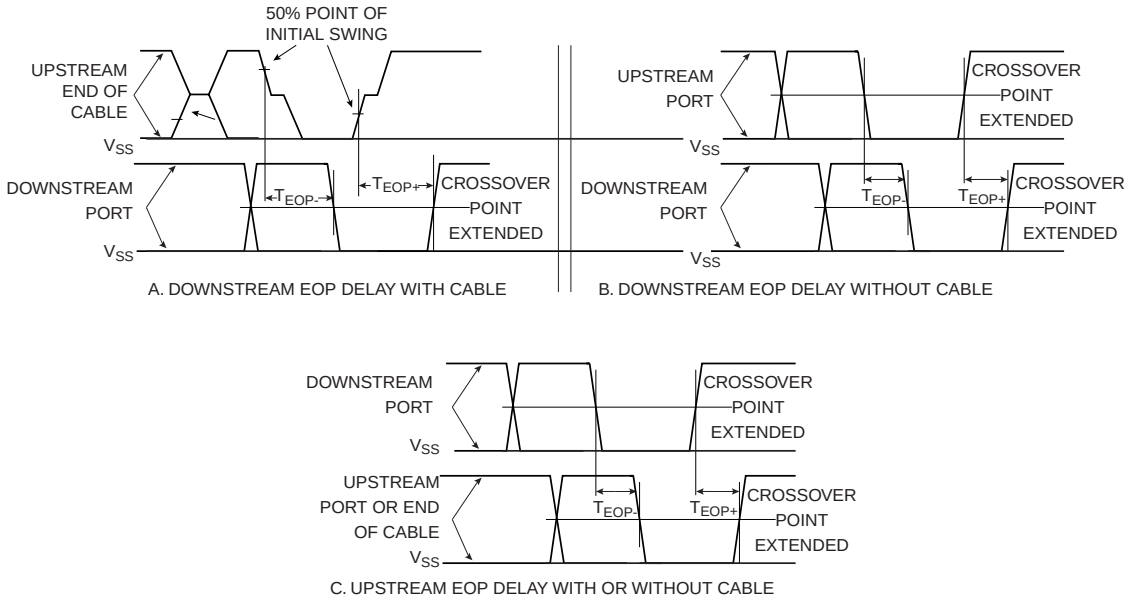


Table 14. Hub Event Timings

Symbol	Parameter	Condition	Min	Max	Unit
t_{DCNN}	Time to Detect a Downstream Port Connect Event Awake Hub Suspended Hub		 2.5 2.5	 2000 12000	 µs µs
t_{DDIS}	Time to Detect a Disconnect Event and Downstream Port Awake Hub Suspended Hub		 2.5 2.5	 2.5 10000	 µs µs
t_{URSM}	Time from Detecting Downstream Resume to Rebroadcast			100	µs
t_{DRST}	Duration of Driving Reset to a Downstream Device	Only for a SetPortFeature (PORT_RESET) request	10	20	ms
t_{URLK}	Time to Detect a Long K From Upstream		2.5	100	µs
t_{URLSEO}	Time to Detect a Long SEO From Upstream		2.5	10,000	µs
t_{URPSEO}	Time of repeating SEO Upstream			23	FS bit time

Figure 13. AT43312A Self-powered USB Hub

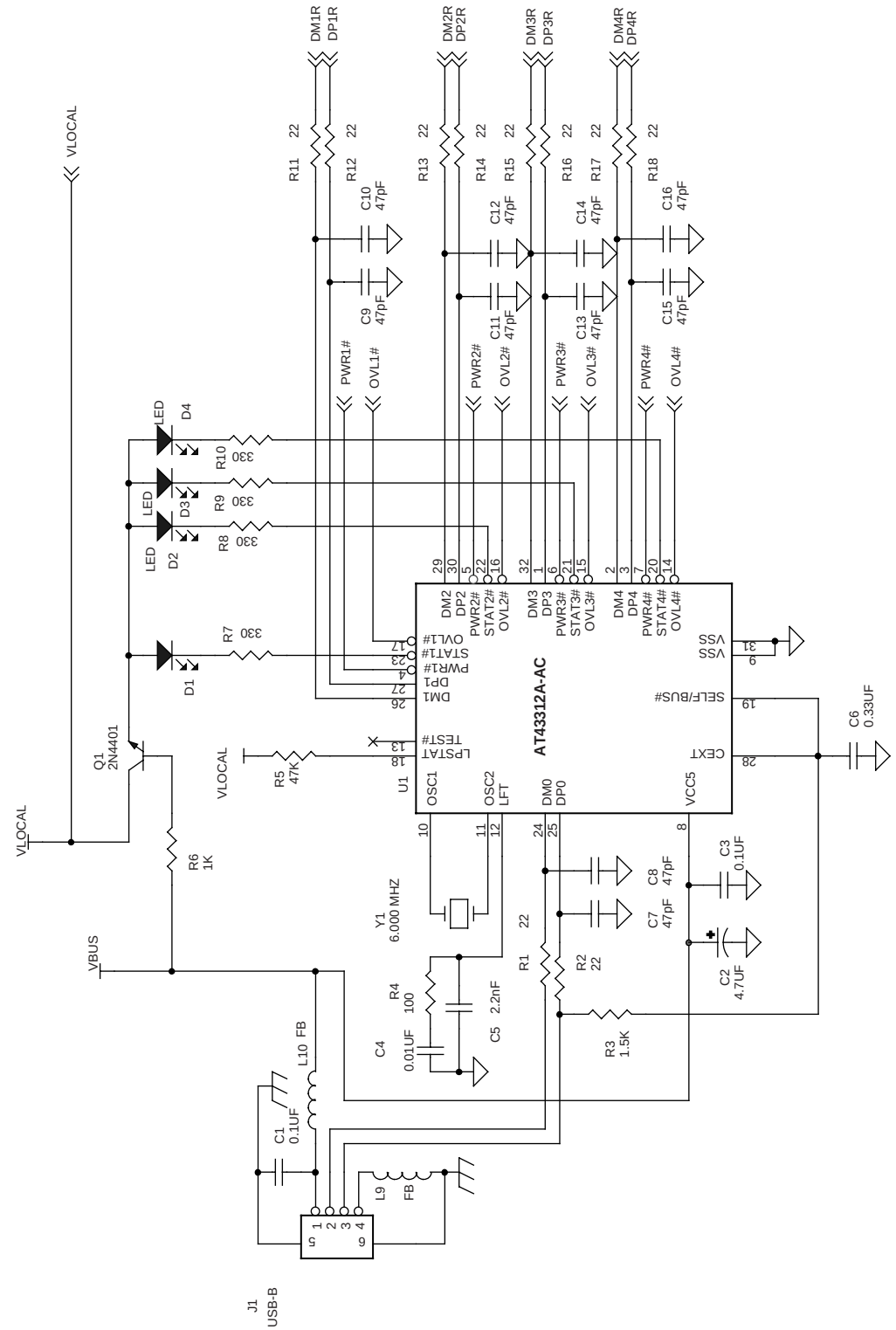


Figure 14. AT43312A Self-powered USB Hub

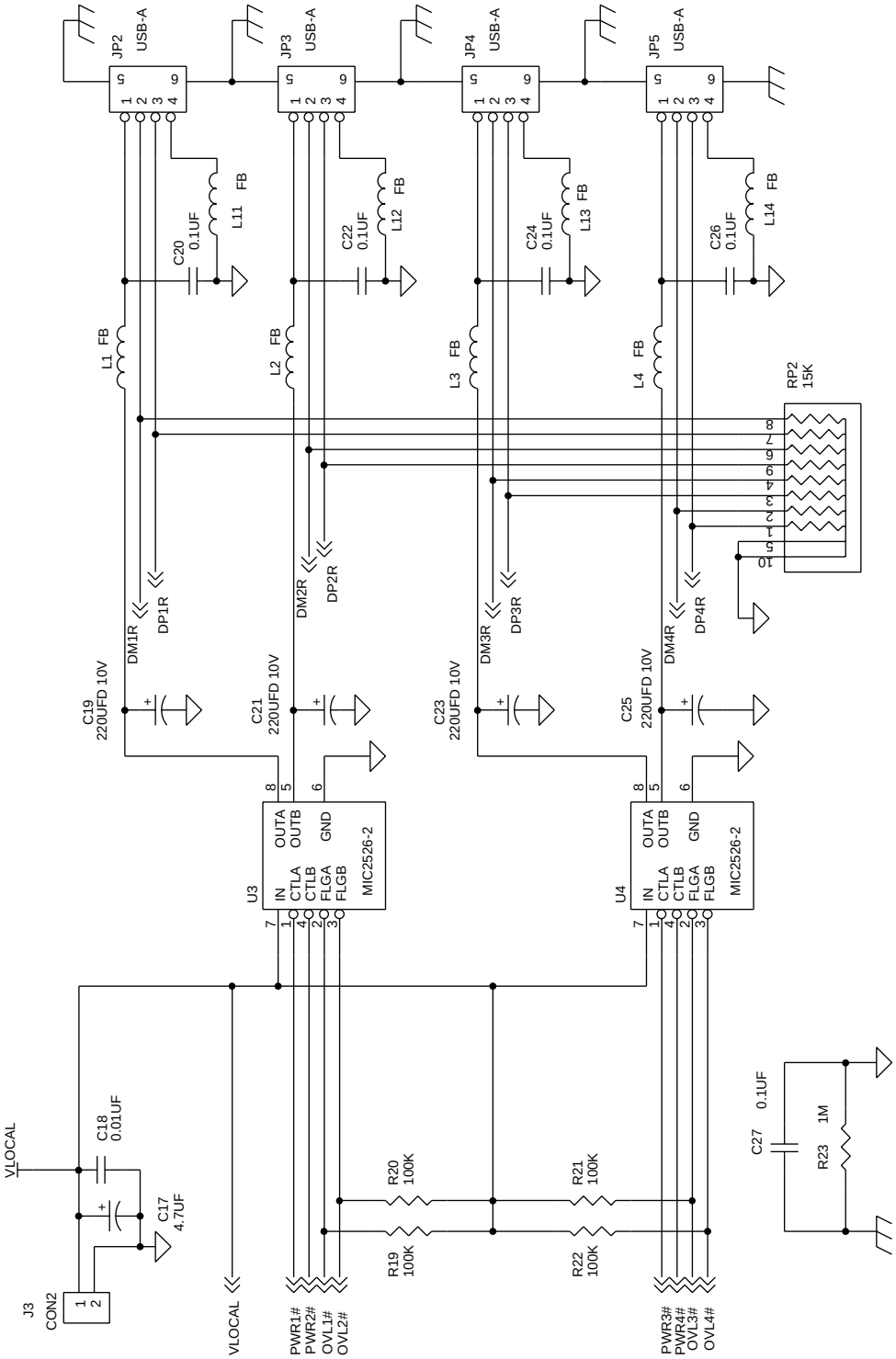


Figure 15. AT43312A Bus-powered USB Hub

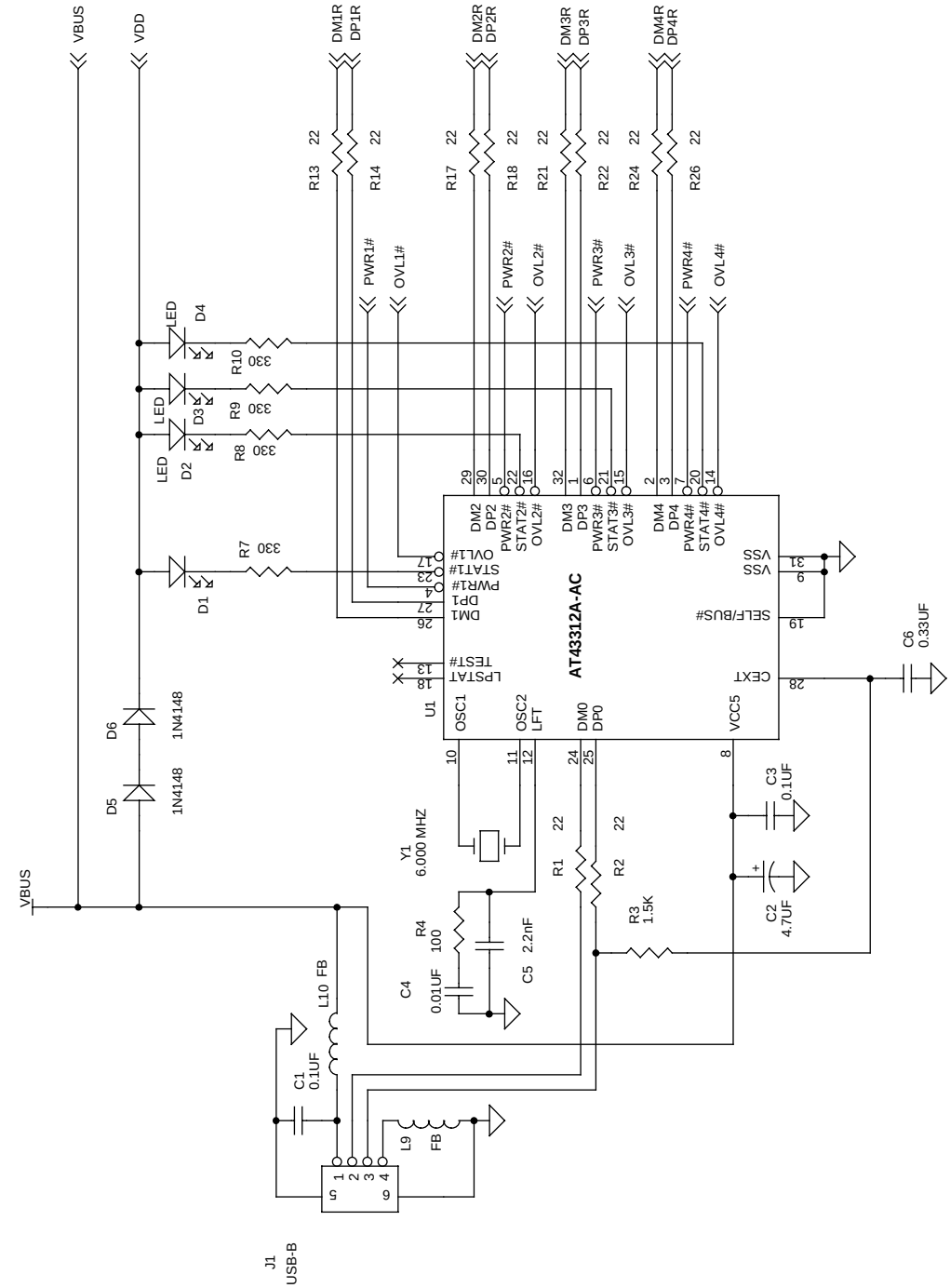
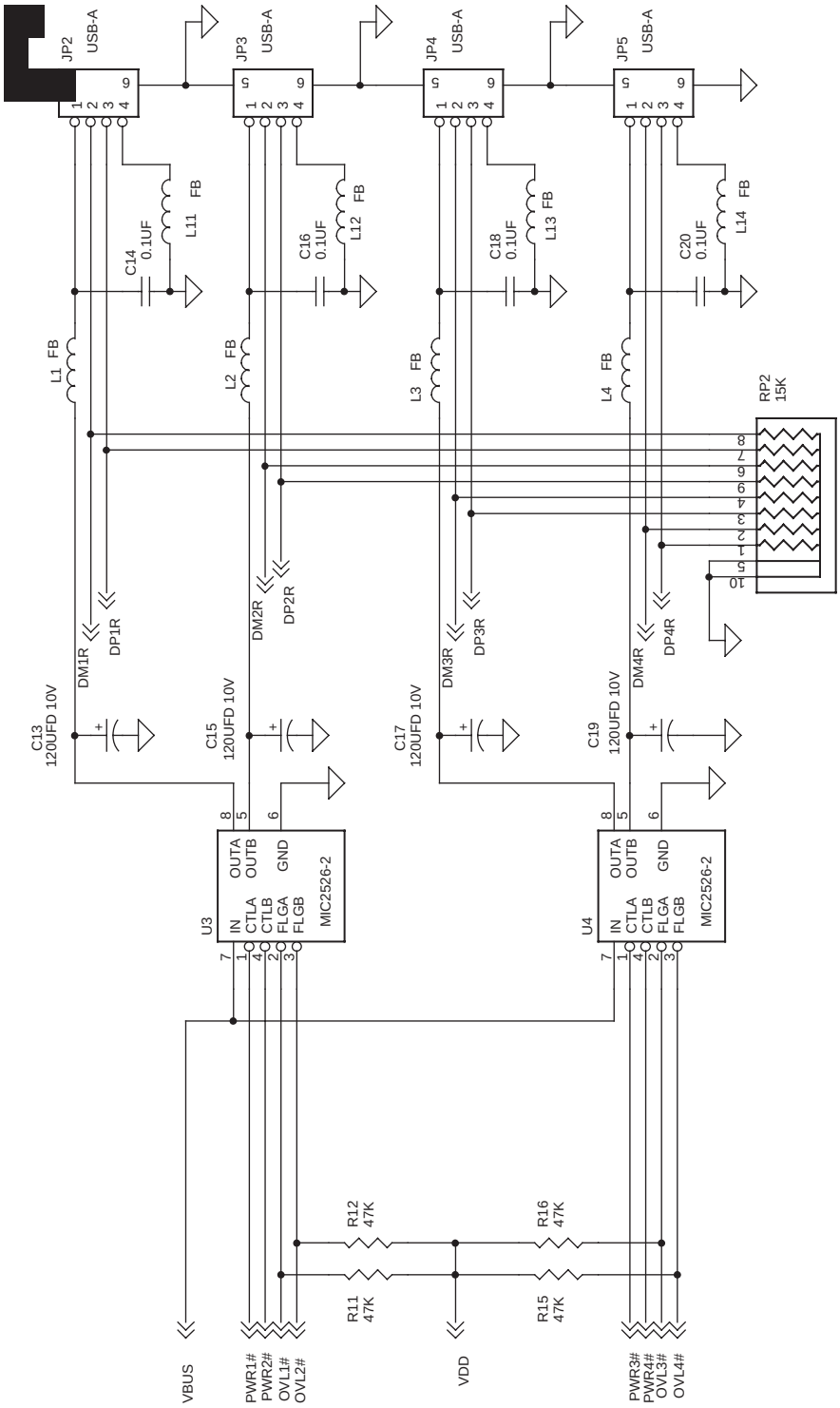


Figure 16. AT43312A Bus-powered USB Hub



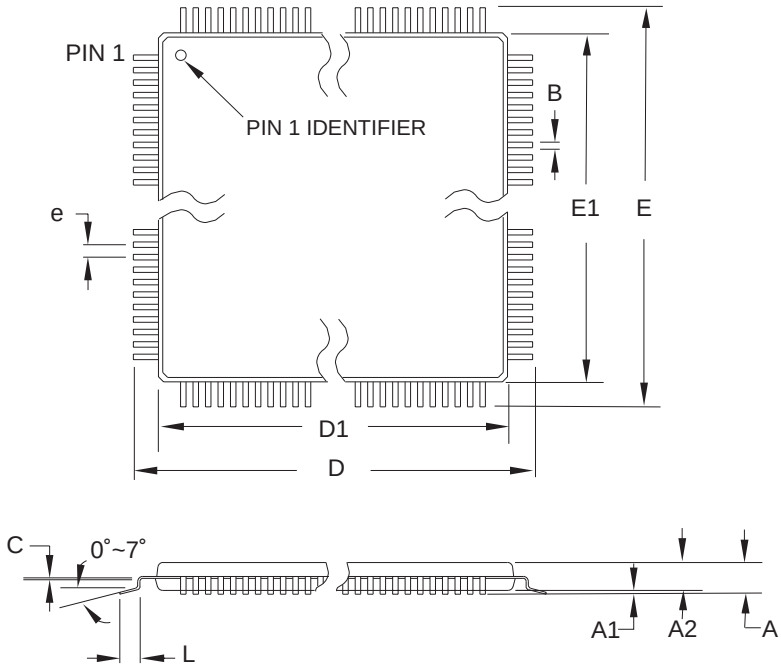
Ordering Information

Ordering Code	Package	Operating Range
AT43312A-AC	32AA	Commercial
AT43312A-SC	32R	(0°C to 70°C)

Package Type	
32AA	32-lead, Low-profile (1.4 mm) Plastic Quad Flat Package (LQFP)
32R	32-lead, 0.440" Wide, Plastic Gull Wing Small Outline (SOIC)

Package Information

32AA – LQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

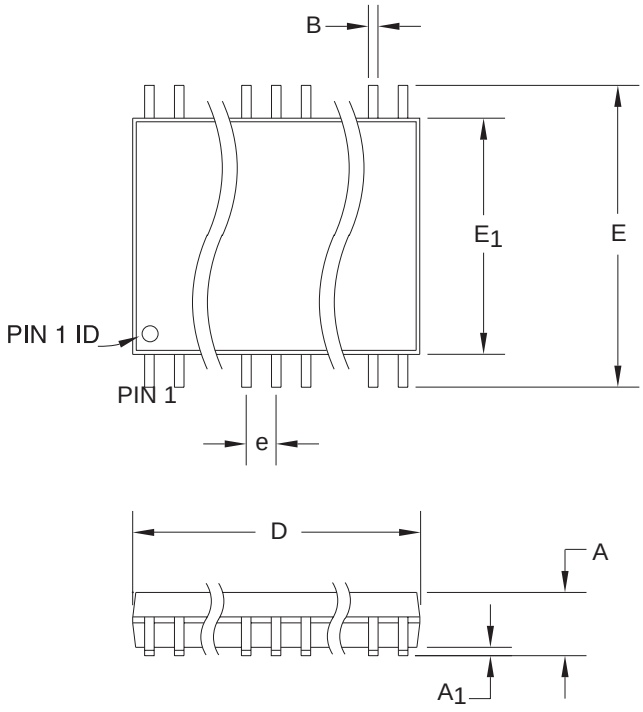
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	1.35	1.40	1.45	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation BBA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32AA,** 32-lead, 7 x 7 mm Body Size, 1.4 mm Body Thickness, 0.8 mm Lead Pitch, Low Profile Plastic Quad Flat Package (LQFP)	32AA	B

32R – SOIC



Note: 1. Dimensions D and E do not include mold Flash or protrusion. Mold Flash or protrusion shall not exceed 0.25 mm (0.010").

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.29	–	2.54	
A1	0.102	–	0.254	
D	20.83	–	21.08	Note 1
E	14.05	–	14.40	
E1	11.05	–	11.30	Note 1
B	0.356	–	0.508	
C	0.1	–	0.22	
L	0.53	–	1.04	
e	1.27 TYP			

06/04/2002

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32R,** 32-lead, 0.440" Body Width, Plastic Gull Wing Small Outline (SOIC)	32R	B

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