



dsPIC30F PROGRAMMER'S REFERENCE MANUAL

dsPIC30F Programmer's Reference Manual Errata Sheet

The dsPIC30F Programmer's Reference Manual (DS70030E) conforms to the information provided in the manual, except for the anomalies described below.

All of the issues listed will be addressed in future releases of the Programmer's Reference Manual.

1. Moving Data with WREG

To clarify how the WREG may be used to move data, the following new section should be added:

4.10.3.3 Moving Data with WREG

The "MOV{.B} f {,WREG}" instruction (described on page 5-145) and "MOV{.B} WREG, f" instruction (described on page 5-146) allow for byte or word data to be moved between file register memory and the WREG (working register W0). These instructions provide equivalent functionality to the legacy Microchip PICmicro MOVF and MOVWF instructions.

The "MOV{.B} f {,WREG}" and "MOV{.B} WREG, f" instructions are the only MOV instructions which support moves of byte data to and from file register memory. Example 4-17 shows several MOV instruction examples using the WREG.

Note: When moving word data between file register memory and the working register array, the "MOV Wns, f" and "MOV f, Wnd" instructions allow any working register (W0:W15) to be used as the source or destination register, not just WREG.

Example 4-17: Moving Data with WREG

```
MOV.B 0x1001, WREG ; move the byte stored at location 0x1001 to W0
MOV    0x1000, WREG ; move the word stored at location 0x1000 to W0
MOV.B WREG, TBLPAG ; move the byte stored at W0 to the TBLPAG register
MOV    WREG, 0x804 ; move the word stored at W0 to location 0x804
```

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2. Instruction Description - Bit Clear f Example 2

On page 5-29, Example 2 for the Bit Clear f instruction should be as follows:

Example 2	BCLR	0x400, #0x9	; Clear bit 9 in 0x400
	Before Instruction		After Instruction
Data 0400	AA55	Data 0400	A855
SR	0000	SR	0000

3. Instruction Description - Computed Branch Example 1

On page 5-32, Example 1 for the Computed Branch instruction should be as follows:

Example 1	002000	HERE:	BRA W7	; Branch forward (2+2*W7)
	002002		. . .	
	
	
	002108		. . .	
	00210A	TABLE7:	. . .	
	00210C		. . .	
	Before Instruction		After Instruction	
PC	00 2000	PC	00 210A	
W7	0084	W7	0084	
SR	0000	SR	0000	

4. Instruction Description Euclidean Distance (No Accumulate) - Status Affected

On page 5-111, the Status Affected for the Euclidean Distance (No Accumulate) instruction should be as follows:

OA, OB, OAB, SA, SB, SAB

5. Instruction Description - Move f to Destination

On page 5-145, the following third note should be added to the Move f to Destination description:

- 3: When moving word data from file register memory, the "MOV f to Wnd" instruction allows any working register (W0:W15) to be the destination register.

6. Instruction Description - Move WREG to f

On page 5-146, the following third note should be added to the Move WREG to f description:

- 3: When moving word data from the working register array to file register memory, the "MOV Wns to f" instruction allows any working register (W0:W15) to be the source register.

7. Instruction Description - Move f to Wnd

On page 5-147, the following third note should be added to the Mov f to Wnd description:

- 3: To move a byte of data from file register memory, the "MOV f to Destination" instruction (page 5-145) may be used.

8. Instruction Description - Move Wns to f

On page 5-148, the following third note should be added to the Mov Wns to f description:

- 3: To move a byte of data to file register memory, the "MOV WREG to f" instruction (page 5-146) may be used.

9. Table 6-3, Instruction "CP0 f" - Status Bits

In Table 6-3, dsPIC30F Instruction Set Summary Table, the "CP0 f" instruction on page 6-12, the "C" and "DC" columns should be as follows:

"1"

10. Table 6-3, Instruction "CP0 Ws" - Status Bits

In Table 6-3, dsPIC30F Instruction Set Summary Table, the "CP0 Ws" instruction on page 6-12, the "C" and "DC" columns should be as follows:

"1"

11. Table 6-3, Instruction "DIV.U Wm, Wn" - Status Bits

In Table 6-3, dsPIC30F Instruction Set Summary Table, the "DIV.U Wm, Wn" instruction on page 6-12, the "OV" column should be as follows:

"0"

12. Table 6-3, Instruction "ED Wm*Wm, Acc, Wx, Wy, Wxd" - Status Bits

In Table 6-3, dsPIC30F Instruction Set Summary Table, the "ED Wm*Wm, Acc, Wx, Wy, Wxd" instruction on page 6-12, the "OA", "OB", "OAB", "SA", "SB" and "SAB" columns should be as follows:

OA, OB, OAB: "↕"

SA, SB, SAB: "↑"

13. Table 6-3, Instruction "LSR f {,WREG}" - Status Bits

In Table 6-3, dsPIC30F Instruction Set Summary Table, the "LSR f {,WREG}" instruction on page 6-13, the "N" column should be as follows:

"0"

14. Table 6-3, Instruction "LSR Ws, Wd" - Status Bits

In Table 6-3, dsPIC30F Instruction Set Summary Table, the "LSR Ws, Wd" instruction on page 6-13, the "N" column should be as follows:

"0"

15. Table 6-3, Instruction "MPY Wm*Wn, Acc, Wx, Wxd, Wy, Wxd" - Status Bits

In Table 6-3, dsPIC30F Instruction Set Summary Table, the "MPY Wm*Wn, Acc, Wx, Wxd, Wy, Wxd" instruction on page 6-13, the "OA", "OB", "OAB", "SA", "SB" and "SAB" columns should be as follows:

OA, OB, OAB: "↕"

SA, SB, SAB: "↑"

16. Table 6-3, Instruction "MPY Wm*Wm, Acc, Wx, Wxd, Wy, Wxd" - Status Bits

In Table 6-3, dsPIC30F Instruction Set Summary Table, the "MPY Wm*Wm, Acc, Wx, Wxd, Wy, Wxd" instruction on page 6-13, the "OA", "OB", "OAB", "SA", "SB" and "SAB" columns should be as follows:

OA, OB, OAB: "↕"

SA, SB, SAB: "↑"

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APPENDIX A: REVISION HISTORY

Revision A (10/2003)

Original version of the document.

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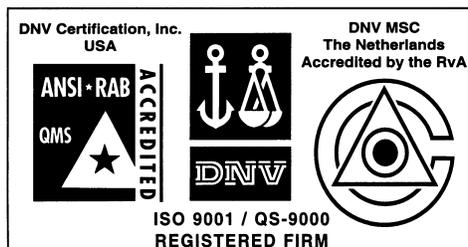
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