BLM7G1822S-80PB; BLM7G1822S-80PBG

LDMOS 2-stage power MMIC

Rev. 2 — 1 September 2015

AMPLEON

Product data sheet

1. Product profile

1.1 General description

The BLM7G1822S-80PB(G) is a dual section, 2-stage power MMIC using Ampleon's state of the art GEN7 LDMOS technology. This multiband device is perfectly suited as general purpose driver or small cell final in the frequency range from 1805 MHz to 2170 MHz. Available in gull wing or straight lead outline.

Table 1. Performance

Typical RF performance at T_{case} = 25 °C. Test signal: 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF; per section unless otherwise specified in a class-AB production circuit.

Test signal	f	I_{Dq1} [1]	I_{Dq2} [1]	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
single carrier W-CDMA	2167.5	80	240	28	8	28	24	–36

[1] I_{Dq1} represents driver stage; I_{Dq2} represents final stage.

1.2 Features and benefits

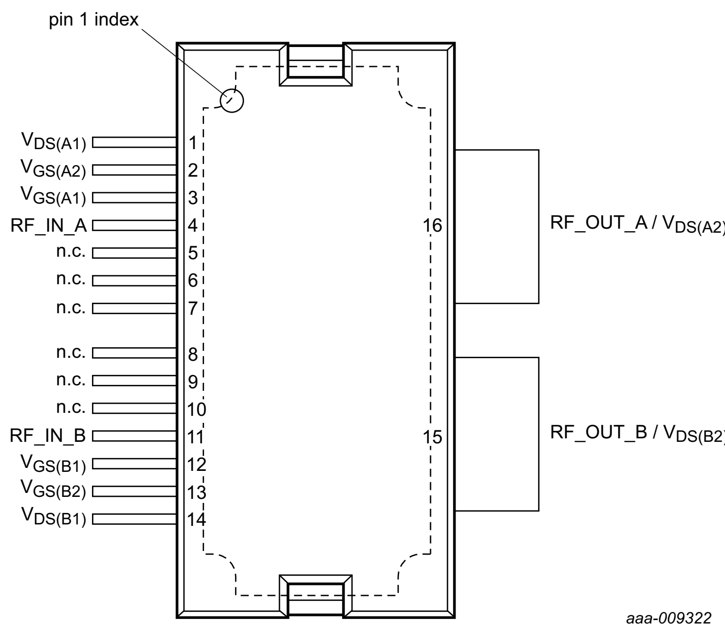
- Designed for broadband operation (frequency 1805 MHz to 2170 MHz)
- High section-to-section isolation enabling multiple combinations
- Integrated temperature compensated bias
- Biasing of individual stages is externally accessible
- Integrated ESD protection
- Excellent thermal stability
- High power gain
- On-chip matching for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- RF power MMIC for W-CDMA base stations in the 1805 MHz to 2170 MHz frequency range. Possible circuit topologies are the following as also depicted in Section 8.1:
  - Dual section or single ended
  - Doherty
  - Quadrature combined
  - Push-pull

2. Pinning information

2.1 Pinning



Transparent top view

The exposed backside of the package is the ground terminal of the device.

Fig 1. Pin configuration

2.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$V_{DS(A1)}$	1	drain-source voltage of section A, driver stage (A1)
$V_{GS(A2)}$	2	gate-source voltage of section A, final stage (A2)
$V_{GS(A1)}$	3	gate-source voltage of section A, driver stage (A1)
RF_IN_A	4	RF input section A
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
n.c.	9	not connected
n.c.	10	not connected
RF_IN_B	11	RF input section B
$V_{GS(B1)}$	12	gate-source voltage of section B, driver stage (B1)
$V_{GS(B2)}$	13	gate-source voltage of section B, final stage (B2)
$V_{DS(B1)}$	14	drain-source voltage of section B, driver stage (B1)

Table 2. Pin description *...continued*

Symbol	Pin	Description
RF_OUT_B/$V_{DS(B2)}$	15	RF output section B / drain-source voltage of section B, final stage (B2)
RF_OUT_A/$V_{DS(A2)}$	16	RF output section A / drain-source voltage of section A, final stage (A2)
GND	flange	RF ground

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLM7G1822S-80PB	HSOP16F	plastic, heatsink small outline package; 16 leads(flat)	SOT1211-2
BLM7G1822S-80PBG	HSOP16	plastic, heatsink small outline package; 16 leads	SOT1212-2

4. Block diagram

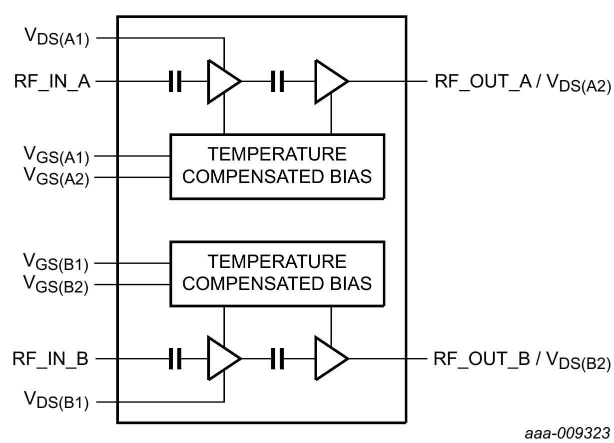


Fig 2. Block diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature		-	150	°C

[1] Continuous use at maximum temperature will affect the reliability. For details refer to the online MTF calculator.

6. Thermal characteristics

Table 5. Thermal characteristics
Measured for total device.

Symbol	Parameter	Conditions		Value	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	final stage; T_{case} = 90 °C; P_L = 5.04 W	[1]	0.8	K/W
		driver stage; T_{case} = 90 °C; P_L = 5.04 W	[1]	2.8	K/W

[1] When operated with a CW signal.

7. Characteristics

Table 6. DC characteristics
T_{case} = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Final stage							
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.604 mA		65	-	-	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 240 mA		1.6	2.0	2.5	V
		V_{DS} = 28 V; I_D = 240 mA	[1]	2.1	2.8	3.6	V
$\Delta I_{Dq}/\Delta T$	quiescent drain current variation with temperature	–40 °C ≤ T_{case} ≤ +85 °C	[1]	-	2	-	%
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V		-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = 5.65 V; V_{DS} = 10 V		-	11	-	A
I_{GSS}	gate leakage current	V_{GS} = 1.0 V; V_{DS} = 0 V		-	-	140	nA
Driver stage							
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.116 mA		65	-	-	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 80 mA		1.7	2.1	2.6	V
		V_{DS} = 28 V; I_D = 80 mA	[2]	2.1	2.7	3.4	V
$\Delta I_{Dq}/\Delta T$	quiescent drain current variation with temperature	–40 °C ≤ T_{case} ≤ +85 °C	[2]	-	2	-	%
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V		-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = 5.65 V; V_{DS} = 10 V		-	1.9	-	A
I_{GSS}	gate leakage current	V_{GS} = 1.0 V; V_{DS} = 0 V		-	-	140	nA

[1] In production circuit with 1205 Ω gate feed resistor.

[2] In production circuit with 460 Ω gate feed resistor.

Table 7. RF Characteristics
Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 80 mA (driver stage); $P_{L(AV)}$ = 8 W unless otherwise specified, measured in an Ampleon straight lead production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Test signal: single carrier W-CDMA [1]						
G_p	power gain	f = 1877.5 MHz; I_{Dq2} = 200 mA (final stage)	-	29	-	dB
		f = 2167.5 MHz; I_{Dq2} = 240 mA (final stage)	26.5	28	29.5	dB
η_D	drain efficiency	f = 1877.5 MHz; I_{Dq2} = 200 mA (final stage)	-	26	-	%
		f = 2167.5 MHz; I_{Dq2} = 240 mA (final stage)	18	24	-	%

Table 7. RF Characteristics *...continued*

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq1} = 80 mA (driver stage); $P_{L(AV)}$ = 8 W unless otherwise specified, measured in an Ampleon straight lead production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RL_{in}	input return loss	f = 1877.5 MHz; I_{Dq2} = 200 mA (final stage)	-	–18	-	dB
		f = 2167.5 MHz; I_{Dq2} = 240 mA (final stage)	-	–20	–10	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	f = 1877.5 MHz; I_{Dq2} = 200 mA (final stage)	-	–38	-	dBc
		f = 2167.5 MHz; I_{Dq2} = 240 mA (final stage)	-	–36	–28.5	dBc
PAR_O	output peak-to-average ratio	f = 1877.5 MHz; I_{Dq2} = 200 mA (final stage)	-	8.6	-	dB
		f = 2167.5 MHz; I_{Dq2} = 240 mA (final stage)	4.6	7	-	dB
Test signal: CW [2]						
$\Delta\varphi_{s21}$	phase response difference	between sections	–15	-	+15	deg
$\Delta\lvert s_{21}\rvert^2$	insertion power gain difference	between sections	–0.6	-	+0.6	dB

[1] 3GPP test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability on CCDF.

[2] f = 2170 MHz.

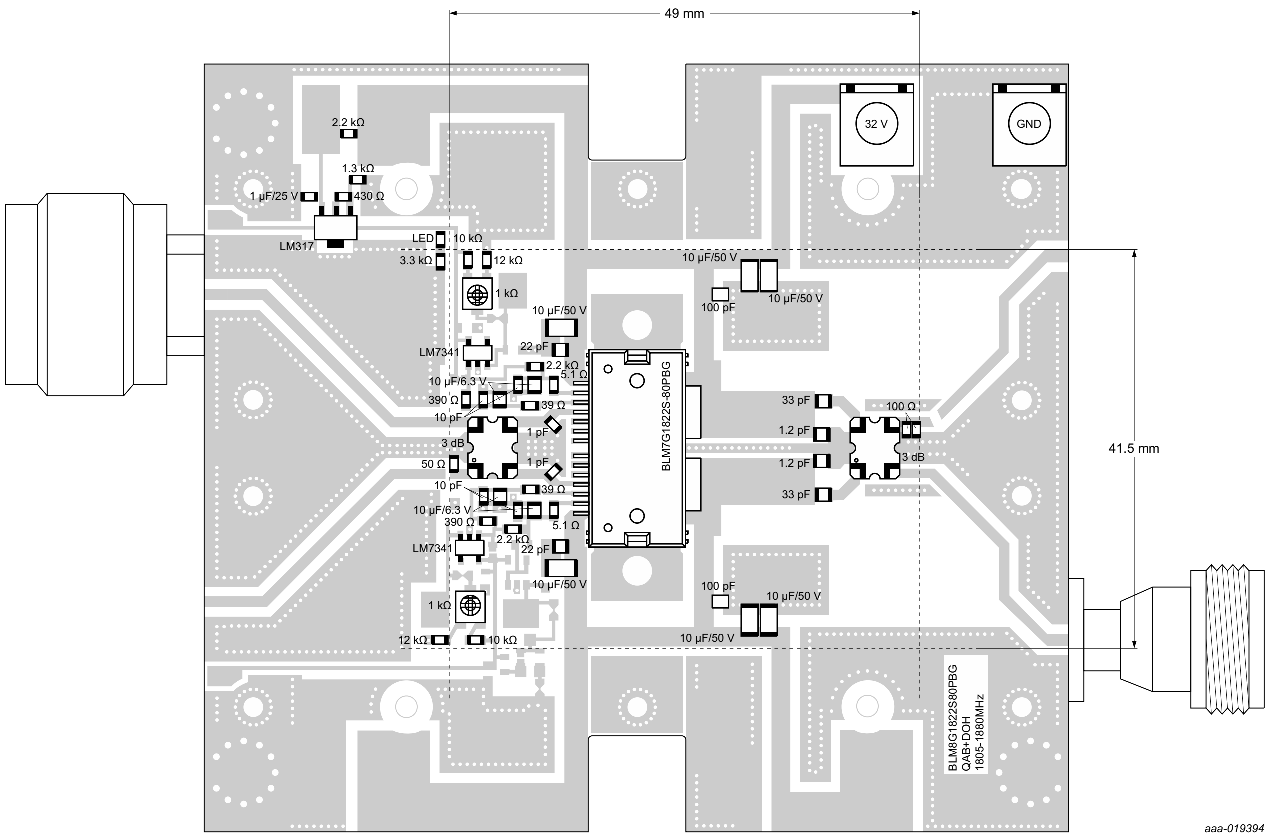
8. Application information

Table 8. Typical performance

T_{case} = 25 °C; V_{DS} = 32 V; I_{Dq} = 544 mA (driver and final stages); Test signal: 1-carrier W-CDMA; 64 DPCH; PAR = 9.9 dB at 0.01 % probability CCDF; unless otherwise specified, measured in an Ampleon, f = 1805 MHz to 1880 MHz, quadrature combined Class AB application circuit (see Figure 3 and Figure 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(1dB)}$	output power at 1 dB gain compression	f = 1840 MHz	-	48.9	-	dBm
$P_{L(3dB)}$	output power at 3 dB gain compression	f = 1840 MHz	-	49.6	-	dBm
η_D	drain efficiency	12 dB OBO ($P_{L(AV)}$ = 37.6 dBm); f = 1840 MHz	-	13.7	-	%
G_p	power gain	$P_{L(AV)}$ = 37.6 W; f = 1840 MHz	-	29	-	dB
B_{video}	video bandwidth	$P_{L(AV)}$ = 41.6 W; 2-tone CW; f = 1840 MHz	-	90	-	MHz
G_{flat}	gain flatness	$P_{L(AV)}$ = 37.6 W	-	0.2	-	dB
$\Delta G/\Delta T$	gain variation with temperature	f = 1840 MHz [1]	-	0.04	-	dB/°C
$\lvert s_{12}\rvert^2$	isolation	between sections A and B; $P_{L(AV)}$ = 9 dBm; f = 1840 MHz; measured on production board; I_{Dq} = 560 mA (both sections)	-	25	-	dB
K	Rollett stability factor	T_{case} = –40 °C; f = 0.1 GHz to 3 GHz [1]	-	> 1	-	

[1] For both sections (S-parameters measured with load-pull jig).



Printed-Circuit Board (PCB): Rogers 4350; thickness = 0.508 mm.

Fig 3. Component layout

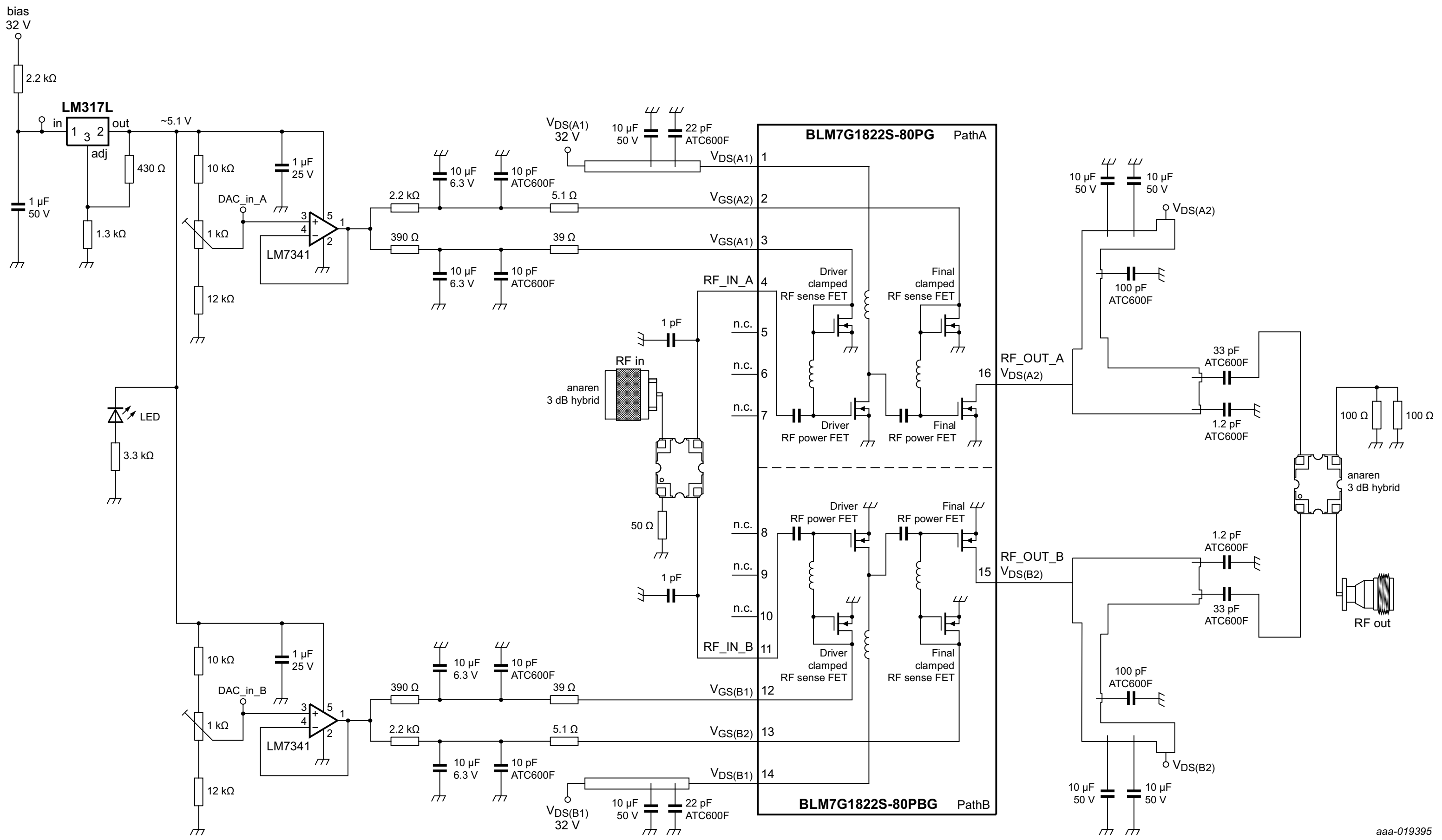


Fig 4. Electrical schematic

8.1 Possible circuit topologies

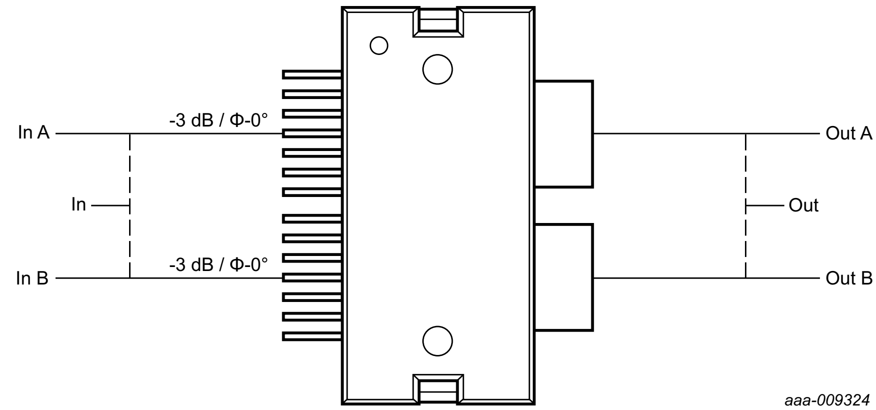


Fig 5. Dual section or single ended

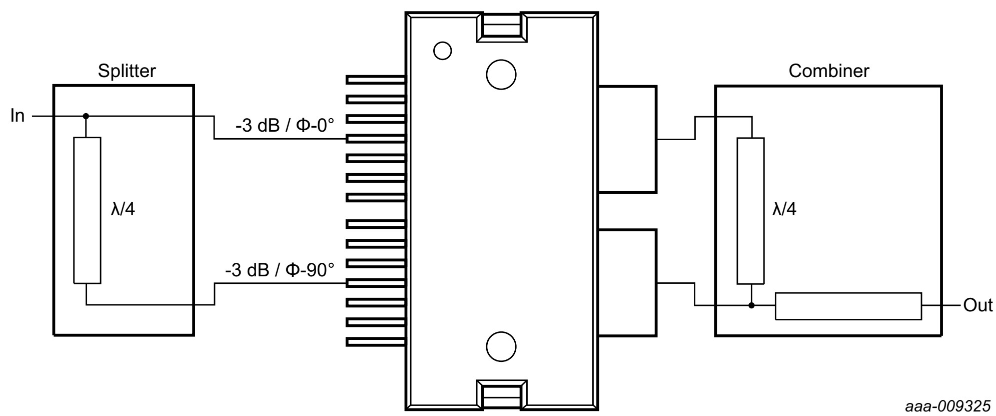


Fig 6. Doherty

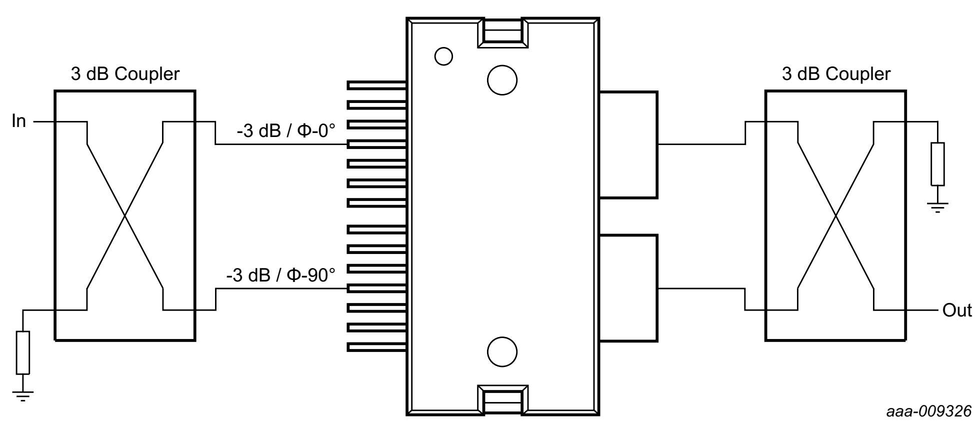


Fig 7. Quadrature combined

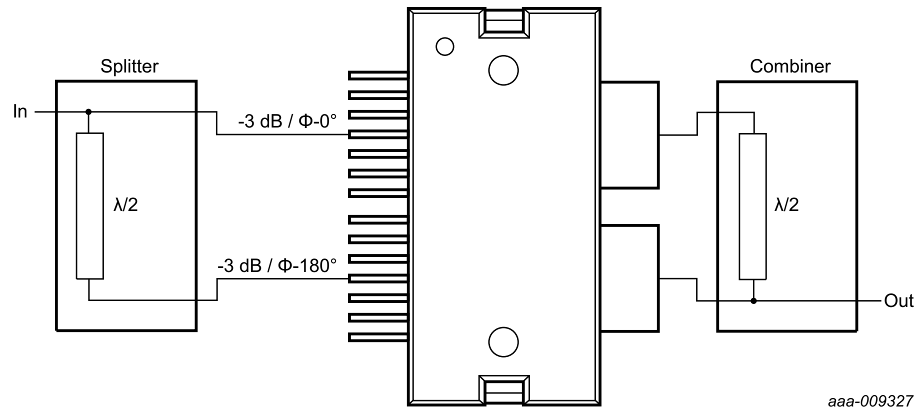


Fig 8. Push-pull

8.2 Ruggedness in class-AB operation

The BLM7G1822S-80PB and BLM7G1822S-80PBG are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: f = 2140 MHz; V_{DS} = 32 V; I_{Dq1} = 80 mA (each section, driver stage); I_{Dq2} = 180 mA (each section, final stage); P_i = 22 dBm (each section). P_i is measured at CW and corresponding to $P_{L(3dB)}$ under Z_S = 50 Ω load.

8.3 Impedance information

Table 9. Typical impedance

Measured load-pull data per section at 3 dB gain compression point; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; t_p = 100 μs; δ = 10 %; Z_S = 50 Ω; I_{Dq1} = 80 mA (driver stage); I_{Dq2} = 200 mA (final stage). Typical values unless otherwise specified.

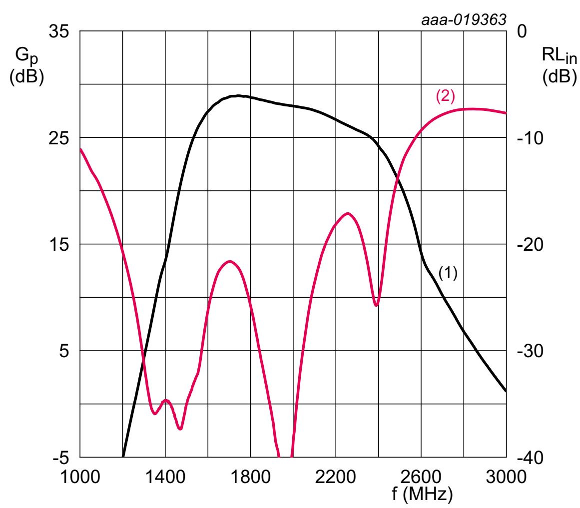
f	tuned for maximum output power					tuned for maximum power added efficiency				
	Z_L	$G_{p(max)}$	P_L	η_{add}	AM-PM conversion	Z_L	$G_{p(max)}$	P_L	η_{add}	AM-PM conversion
(MHz)	(Ω)	(dB)	(W)	(%)	(deg)	(Ω)	(dB)	(W)	(%)	(deg)
BLM7G1822S-80PB										
1810	2.6 – j5.9	29.2	48.6	49.6	–2.7	5.4 – j5.1	30.3	47.4	56.4	–5.6
1840	2.7 – j5.8	29.9	48.5	49.3	–3.8	4.9 – j4.8	30.9	47.5	56.3	–6.2
1880	2.6 – j5.8	29.6	48.5	48.5	–2.4	4.8 – j4.3	30.6	47.4	55.3	–5.0
1930	2.6 – j5.8	29.9	48.4	47.9	–1.1	4.3 – j4.2	30.8	47.4	54.3	–2.9
1960	2.6 – j5.8	29.9	48.4	48.0	–1.0	4.2 – j4.2	30.8	47.5	54.3	–2.2
1990	2.6 – j5.7	29.6	48.3	47.5	–2.1	3.6 – j4.0	30.4	47.4	53.8	–3.9
2110	2.6 – j5.8	29.8	48.3	48.3	–3.6	3.1 – j4.1	30.2	47.4	52.6	–4.7
2140	2.6 – j5.8	29.8	48.3	48.6	–4.1	3.1 – j4.7	30.3	47.6	51.9	–3.9
2170	2.6 – j5.8	29.5	48.2	46.0	–5.4	2.6 – j4.7	30.1	47.5	51.2	–6.4
BLM7G1822S-80PBG										
1810	3.0 – j8.9	29.3	48.4	50.6	–1.7	5.3 – j7.6	30.3	47.5	57.5	–5.3
1840	2.7 – j8.7	29.1	48.3	48.4	–4.4	5.0 – j7.5	30.2	47.5	56.9	–7.5
1880	3.0 – j8.8	29.4	48.4	50.5	–2.3	4.7 – j7.1	30.3	47.4	56.4	–5.1

Table 9. Typical impedance *...continued*

Measured load-pull data per section at 3 dB gain compression point; test signal: pulsed CW; T_{case} = 25 °C; V_{DS} = 28 V; t_p = 100 μs; δ = 10 %; Z_S = 50 Ω; I_{Dq1} = 80 mA (driver stage); I_{Dq2} = 200 mA (final stage). Typical values unless otherwise specified.

f	tuned for maximum output power					tuned for maximum power added efficiency				
	Z_L	$G_{p(max)}$	P_L	η_{add}	AM-PM conversion	Z_L	$G_{p(max)}$	P_L	η_{add}	AM-PM conversion
(MHz)	(Ω)	(dB)	(W)	(%)	(deg)	(Ω)	(dB)	(W)	(%)	(deg)
1930	2.7 – j9.0	29.6	48.4	48.7	–2.7	4.4 – j7.0	30.6	47.4	56.1	–5.5
1960	2.7 – j9.0	29.6	48.4	48.7	–2.7	4.0 – j6.8	30.6	47.4	55.9	–5.3
1990	2.7 – j8.9	29.7	48.4	48.0	–2.0	3.8 – j7.1	30.6	47.5	55.0	–3.7
2110	2.7 – j9.5	29.9	48.5	49.5	–3.4	2.8 – j7.6	30.6	47.6	54.9	–4.2
2140	2.6 – j9.5	29.9	48.3	49.1	–4.0	2.6 – j7.9	30.5	47.6	53.7	–3.2
2170	2.4 – j9.7	29.7	48.3	47.4	–5.5	2.6 – j8.2	30.5	47.7	53.0	–4.6

8.4 Graphs



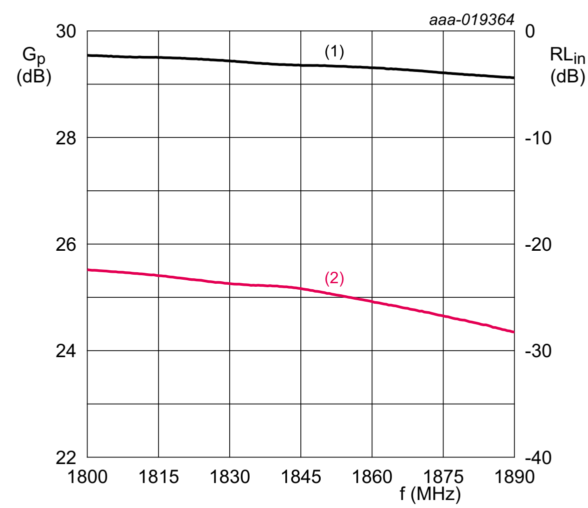
T_{case} = 25 °C; V_{DS} = 32 V; P_L = 1.096 W;
I_{Dq1} + I_{Dq2} = 272 mA (driver and final stages; valid for both sections A and B);
V_{GS} = 2.07 V (driver stage);
V_{GS} = 1.87 V (final stage).

Test signal: CW.

(1) magnitude of G_p

(2) magnitude of RL_{in}

Fig 9. Wideband power gain and input return loss as function of frequency; typical values



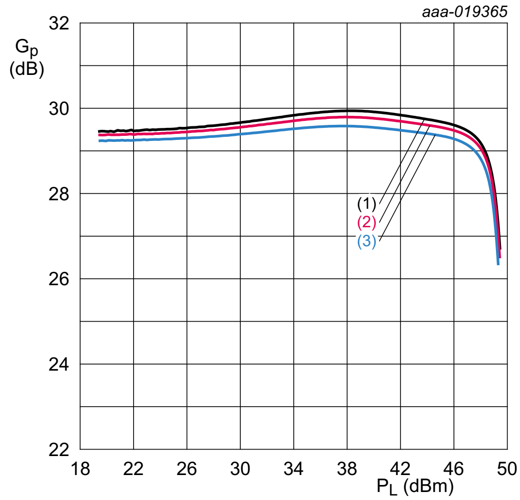
T_{case} = 25 °C; V_{DS} = 32 V; P_L = 3.02 W;
I_{Dq1} + I_{Dq2} = 272 mA (driver and final stages; valid for both sections A and B);
V_{GS} = 2.07 V (driver stage);
V_{GS} = 1.87 V (final stage).

Test signal: CW.

(1) magnitude of G_p

(2) magnitude of RL_{in}

Fig 10. In-band power gain and input return loss as function of frequency; typical values



T_{case} = 25 °C; V_{DS} = 32 V;
$I_{Dq1} + I_{Dq2}$ = 272 mA (driver and final stages; valid for both sections A and B);
V_{GS} = 2.07 V (driver stage);
V_{GS} = 1.87 V (final stage).

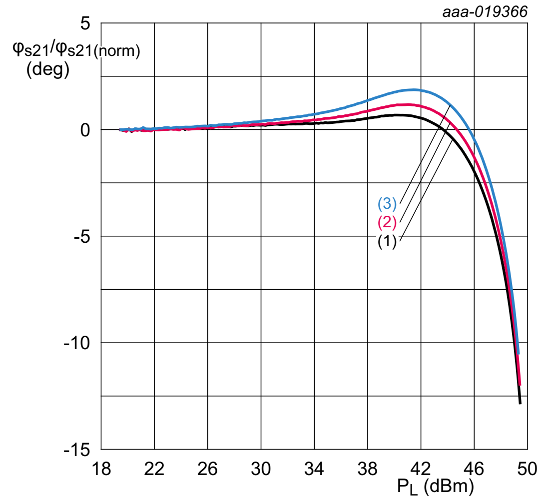
Test signal: pulsed CW.

(1) f = 1805 MHz

(2) f = 1840 MHz

(3) f = 1880 MHz

Fig 11. Power gain as a function of output power; typical values



T_{case} = 25 °C; V_{DS} = 32 V;
$I_{Dq1} + I_{Dq2}$ = 272 mA (driver and final stages; valid for both sections A and B);
V_{GS} = 2.07 V (driver stage);
V_{GS} = 1.87 V (final stage).

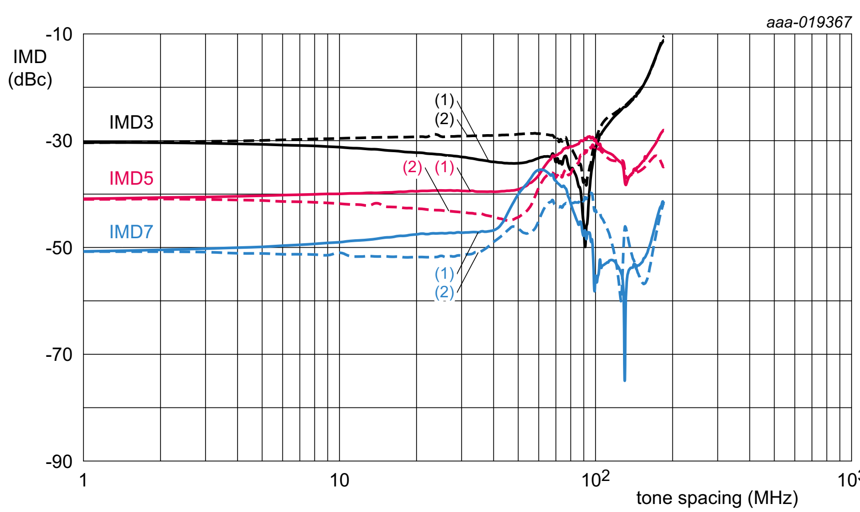
Test signal: pulsed CW.

(1) f = 1805 MHz

(2) f = 1840 MHz

(3) f = 1880 MHz

Fig 12. Normalized phase response as a function of output power; typical values



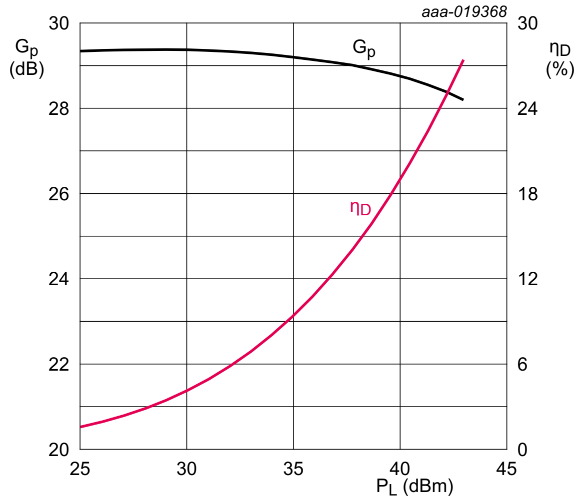
T_{case} = 25 °C; V_{DS} = 32 V; $I_{Dq1} + I_{Dq2}$ = 272 mA (driver and final stages; valid for both sections A and B);
V_{GS} = 2.07 V (driver stage); V_{GS} = 1.87 V (final stage).

Test signal: 2-tone CW; f_c = 1840 MHz.

(1) IMD low

(2) IMD high

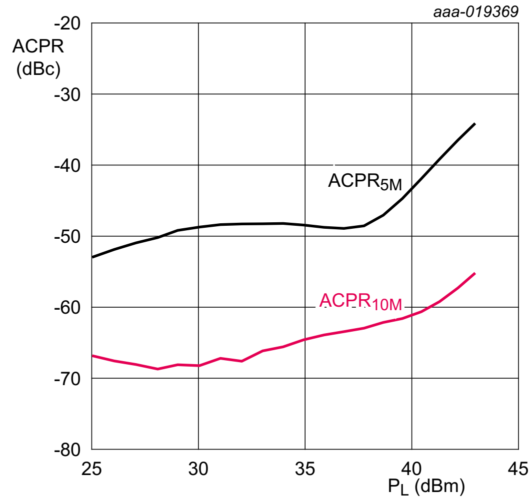
Fig 13. Intermodulation distortion as a function of tone spacing; typical values



T_{case} = 25 °C; V_{DS} = 32 V; f = 1840 MHz;
I_{Dq1} + I_{Dq2} = 272 mA (driver and final stages; valid for both sections A and B);
V_{GS} = 2.07 V (driver stage);
V_{GS} = 1.87 V (final stage).

Test signal: 1-carrier W-CDMA; test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability CCDF.

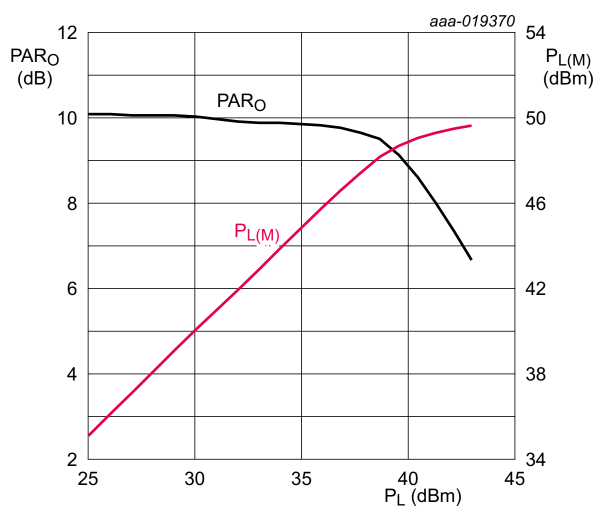
Fig 14. Power gain and drain efficiency as function of output power; typical values



T_{case} = 25 °C; V_{DS} = 32 V; f = 1840 MHz;
I_{Dq1} + I_{Dq2} = 272 mA (driver and final stages; valid for both sections A and B);
V_{GS} = 2.07 V (driver stage);
V_{GS} = 1.87 V (final stage).

Test signal: 1-carrier W-CDMA; test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability CCDF.

Fig 15. Adjacent channel power ratio as a function of output power; typical values



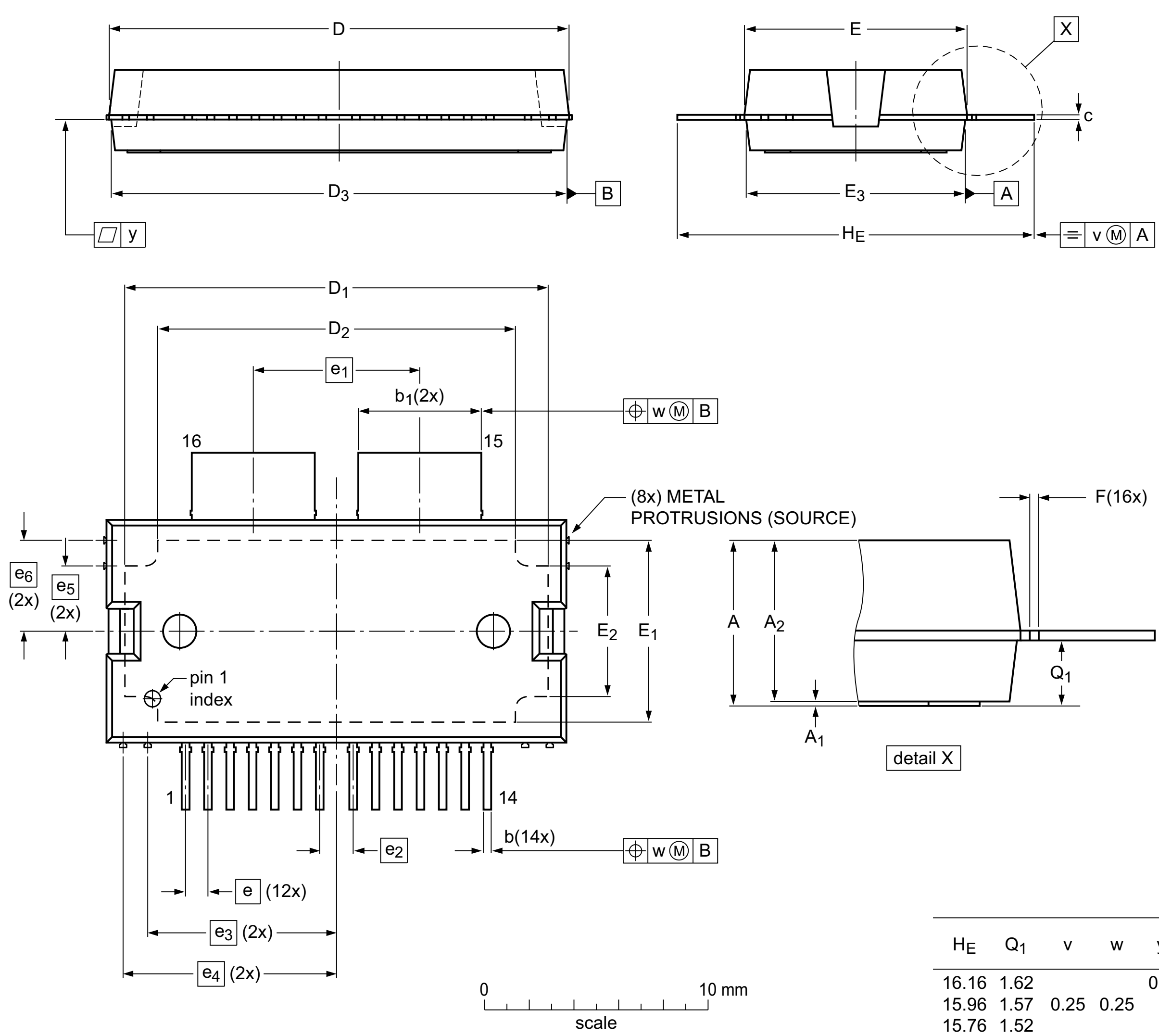
T_{case} = 25 °C; V_{DS} = 32 V; f = 1840 MHz; I_{Dq1} + I_{Dq2} = 272 mA (driver and final stages; valid for both sections A and B);
V_{GS} = 2.07 V (driver stage); V_{GS} = 1.87 V (final stage).

Test signal: 1-carrier W-CDMA; test model 1; 64 DPCH; PAR = 9.9 dB at 0.01 % probability CCDF.

Fig 16. Output peak-to-average ratio and peak output power as function of output power; typical values

9. Package outline

HSOP16F: plastic, heatsink small outline package; 16 leads(flat) **SOT1211-2**



	H_E	Q_1	v	w	y
max	16.16	1.62			0.1
nom	15.96	1.57	0.25	0.25	
min	15.76	1.52			

Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	b_1	c	D(1)	D_1	D_2	D_3	E(1)	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4	e_5	e_6	F
mm	max	3.9	0.2	3.65	0.40	5.55	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83								
	nom		0.1	3.60	0.35	5.50	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	1.0	7.45	1.5	8.45	9.55	2.97	4.07	0.2
	min		0	3.55	0.30	5.45	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73								

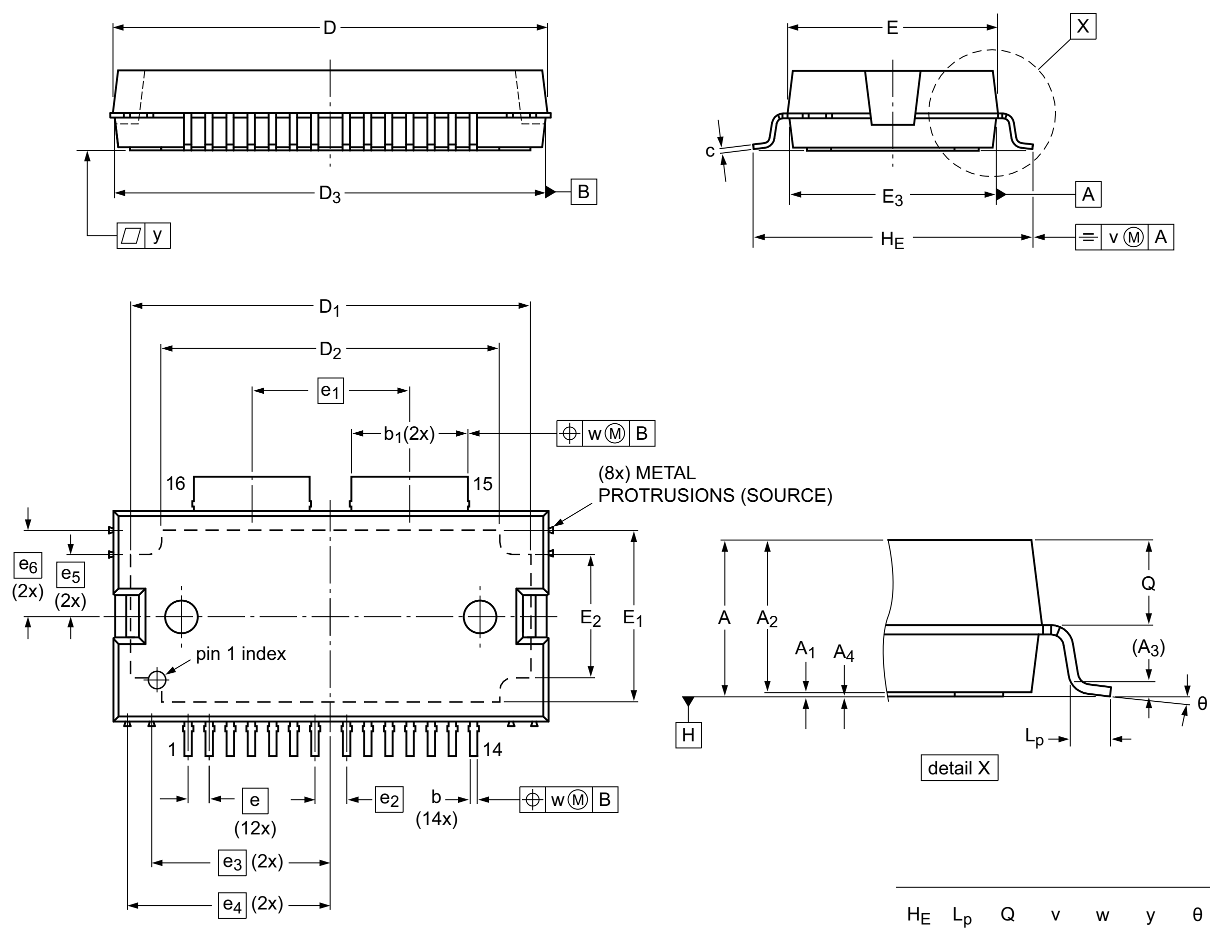
Note
1. Package body dimensions “D and “E do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimensions “b and “ b_1 do not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.

sot1211-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1211-2						~~15-01-12~~ 15-06-09

Fig 17. Package outline SOT1211-2 (HSOP16F)

HSOP16: plastic, heatsink small outline package; 16 leads **SOT1212-2**



0 10 mm
scale

Dimensions (mm are the original dimensions)

H_E	L_p	Q	v	w	y	θ
13.5	1.10	2.07			0.1	7°
13.2	0.95	2.02	0.25	0.25		3°
12.9	0.80	1.97				0°

Unit		A	A_1	A_2	A_3	A_4	b	b_1	c	D(1)	D_1	D_2	D_3	E(1)	E_1	E_2	E_3	e	e_1	e_2	e_3	e_4	e_5	e_6
mm	max	3.9	0.2	3.65		0.06	0.40	5.55	0.27	20.62	19.00	16.05	20.44	10.01	8.18	5.89	9.83							
	nom		0.1	3.60	0.35	0	0.35	5.50	0.22	20.57	18.95	16.00	20.39	9.96	8.13	5.84	9.78	1.0	7.45	1.5	8.45	9.55	2.97	4.07
	min		0	3.55		-0.02	0.30	5.45	0.17	20.52	18.90	15.95	20.34	9.91	8.08	5.79	9.73							

Note
1. Package body dimensions “D" and `'E" do not include mold and metal protrusions. Allowable protrusion is 0.25 mm per side.
2. Lead width dimensions `'b" and `'b1" do not include dambar protrusions. Allowable dambar protrusion is 0.25 mm in total per lead.
3. Dimension A_4 is measured with respect to bottom of the heatsink DATUM H. Positive value means that the bottom of the heatsink is higher than the bottom of the lead.

sot1212-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1212-2						~~15-01-14~~ 15-06-09

Fig 18. Package outline SOT1212-2 (HSOP16)

10. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

11. Abbreviations

Table 10. Abbreviations

Acronym	Description
AM	Amplitude Modulation
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
GEN7	Seventh Generation
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MMIC	Monolithic Microwave Integrated Circuit
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

12. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLM7G1822S-80PB_S-80PBG v.2	20150901	Product data sheet	-	BLM7G1822S-80PB_S-80PBG v.1
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of Ampleon • Legal texts have been adapted to the new company name where appropriate			
BLM7G1822S-80PB_S-80PBG v.1	20150824	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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15. Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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