## Features

- Single- or Dual-Supply Voltage Monitors
- Precision Factory-Set Reset Thresholds from 1.6V to 4.6V
- Adjustable Threshold to Monitor Voltages Down to 0.63V (PT7M7449~7452)
- Single or Dual Manual Reset Inputs with Extended 6.72s Setup Period
- Optional Short Setup Time Manual Reset Input (PT7M7447/7448/7451/7452)
- Immune to Short Voltage Transients
- Low 3μA Supply Current
- Guaranteed Valid Reset Down to $V_{DD}$=1.0V
- Active-Low/RESET (Push-Pull or Open-Drain) Outputs
- 140ms(min) Reset Timeout Period
- Small 5-Pin and 6-Pin SOT23 Packages

## Ordering Information

| Part Number | Package |
|---|---|
| PT7M7443xTAE | lead-free and Green SOT23-5 |
| PT7M7444xTAE | lead-free and Green SOT23-5 |
| PT7M7445xTAE | lead-free and Green SOT23-5 |
| PT7M7446xTAE | lead-free and Green SOT23-5 |
| PT7M7447xTAE | lead-free and Green SOT23-5 |
| PT7M7448xTAE | lead-free and Green SOT23-5 |
| PT7M7449xTAE | lead-free and Green SOT23-6 |
| PT7M7450xTAE | Lead-free and Green SOT23-6 |
| PT7M7451xTAE | lead-free and Green SOT23-6 |
| PT7M7452xTAE | lead-free and Green SOT23-6 |

**Note:** suffix "x" represents 9 kinds of factory trimmed reset threshold voltage. Please see below table.

## Description

The PT7M7443~7452 low-current microprocessor reset circuits feature single or dual manual reset inputs with an extended 6.72s setup period. Because of the extended setup period, short switch closures (nuisance resets) are ignored.

On all devices, the reset output asserts when any of the monitored supply voltages drops below its specified threshold. The reset output remains asserted for the reset timeout period (210ms typ) after all monitored supplies exceed their reset thresholds. The reset output is one-shot pulse asserted for the reset timeout period (140ms min) when selected manual reset input(s) are held low for an extended setup timeout period of 6.72s. These devices ignore manual reset transitions of less than 6.72s (typ).

The PT7M7443~7448 are single fixed-voltage μP supervisors. The PT7M7443/7444 have a single extended manual reset input. The PT7M7445/7446 have two extended manual reset inputs. The PT7M7447/7448 have one extended and one immediate manual reset input.

The PT7M7449~7452 have one fixed-threshold μP supervisor and one adjustable-threshold μP supervisor. The PT7m7449/7450 have two delayed manual reset inputs. The PT7M7451/7452 have one delayed and one immediate manual reset input.

The PT7M7443~7452 have an active-low /RESET with push-pull or open-drain output logic options. These devices, offered in small SOT package, are fully guaranteed over the extended temperature range (-40℃ to +85℃).

## Applications

- Monitoring lithiumion ($Li^+$) cells or multicell alkaline/ NiCd/ NiMH power supplies.

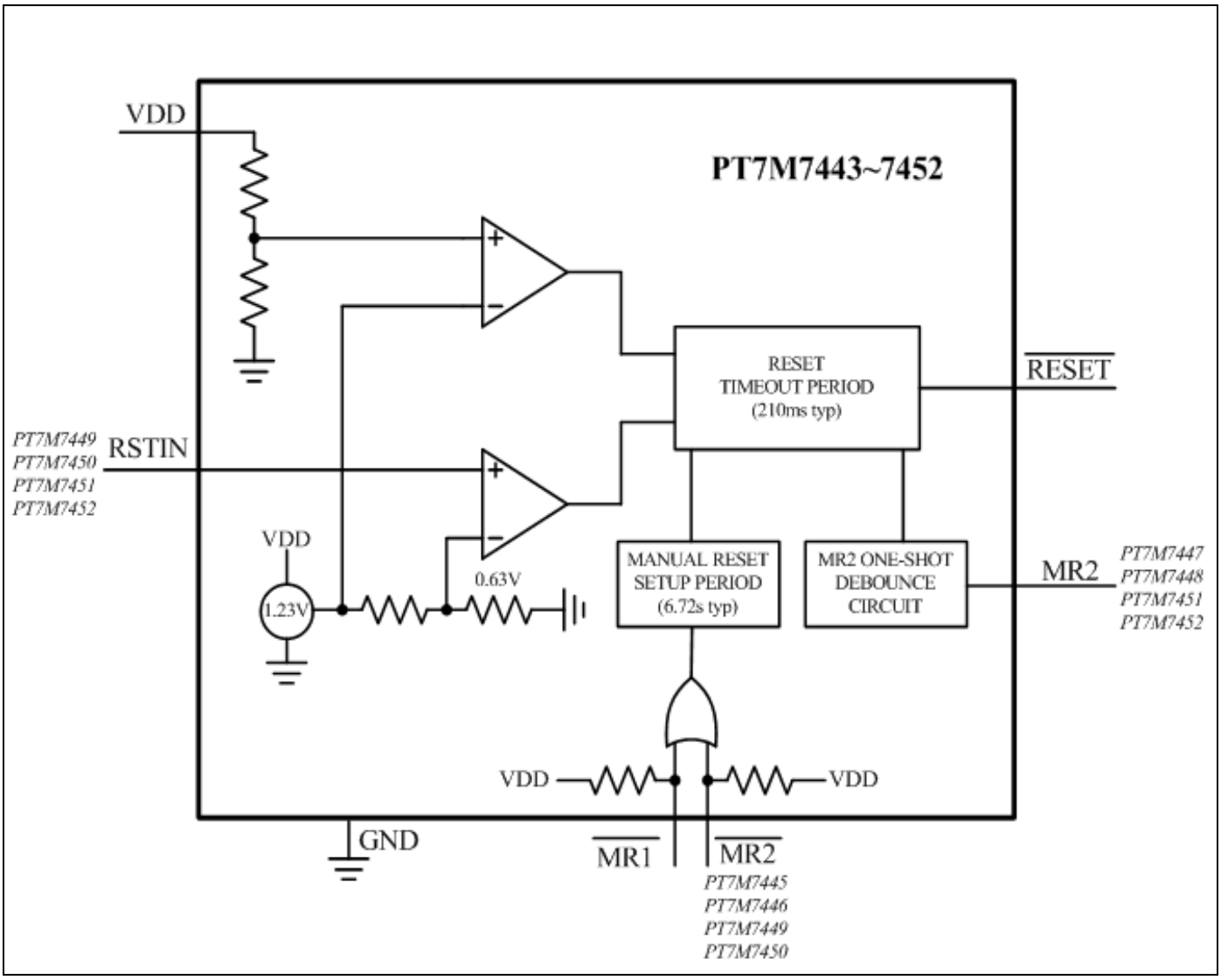
**Table 1** Suffix "x" definition of PT7M7443~7452

| Suffix x | L | M | T | S | R | Z | Y | W | V |
|---|---|---|---|---|---|---|---|---|---|
| Reset threshold (V) | 4.63 | 4.38 | 3.08 | 2.93 | 2.63 | 2.32 | 2.19 | 1.67 | 1.58 |

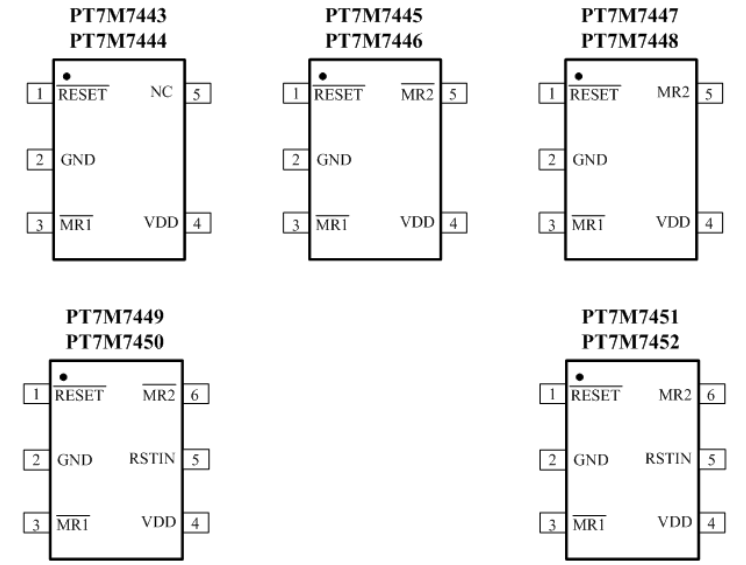
**Table 2** Function comparison of PT7M7443~7452

| PART | Push-Pull Active-Low Output | Open-Drain Active-Low Output | /MR1 Setup | /MR2 Setup | MR2 (No Setup) | RSTIN | Package |
|---|---|---|---|---|---|---|---|
| PT7M7443 | √ | - | 6.72s | - | - | - | SOT23-5 |
| PT7M7444 | - | √ | 6.72s | - | - | - | |
| PT7M7445 | √ | - | 6.72s | 6.72s | - | - | |
| PT7M7446 | - | √ | 6.72s | 6.72s | - | - | |
| PT7M7447 | √ | - | 6.72s | - | √ | - | |
| PT7M7448 | - | √ | 6.72s | - | √ | - | |
| PT7M7449 | √ | - | 6.72s | 6.72s | - | √ | SOT23-6 |
| PT7M7450 | - | √ | 6.72s | 6.72s | - | √ | |
| PT7M7451 | √ | - | 6.72s | - | √ | √ | |
| PT7M7452 | - | √ | 6.72s | - | √ | √ | |

## Block Diagram



## Pin Configuration




## Pin Description

| Pin | | | | | Name | Function |
|---|---|---|---|---|---|---|
| 7443/44 | 7445/46 | 7447/48 | 7449/50 | 7451/52 | | |
| 1 | 2 | 2 | 2 | 2 | GND | **Ground** |
| 3 | 1 | 1 | 1 | 1 | /RESET | **Active-Low Push-Pull or Open-Drain Output.** /RESET changes from high to low when $V_{DD}$ or RSTIN drops below its selected reset threshold and remains low for the 210ms reset timeout period after all monitored power-supply inputs exceed their selected reset thresholds. /RESET is one-shot pulsed low for the reset timeout period (140ms min) after selected manual reset inputs are asserted longer than the specified setup period. For the open-drain output, use a minimum 20kΩ pull-up resistor to $V_{DD}$. |
| 4 | -- | 3 | -- | 3 | /MR1 | **Manual Reset Input, Active Low.** Internal 50kΩ pull-up to VDD. Pull /MR1 low for the typical input pulse width (6.72s) to one-shot pulse /RESET for the reset timeout period. |
| -- | 3 | -- | 3 | -- | | **Manual Reset Input, Active Low.** Pull both /MR1 and /MR2 low for the typical input pulse width (6.72s) to one-shot pulse /RESET for the reset timeout period. |
| 5 | 4 | 4 | 4 | 4 | VDD | **$V_{DD}$ Voltage Input**. Power supply and input for the primary microprocessor voltage reset monitor. |
| -- | 5 | -- | 6 | -- | /MR2 | **Manual Reset Input, Active Low.** Internal 50kΩ pull-up to $V_{DD}$. Pull both /MR1 and /MR2 low for the typical input pulse width (6.72s) to one-shot pulse /RESET for the reset timeout period. |
| -- | -- | 5 | -- | 6 | MR2 | **Manual Reset Input.** Pull theMR2 high to immediately one-shot pulse /RESET for the reset timeout peiod. |
| -- | -- | -- | 5 | 5 | RSTIN | **Reset Input.** High-impedance input to the adjustable reset comparator. Connect RSTIN to the center point of an external resistor-divider to set the threshold of the externally monitored voltage. |
| 2 | -- | -- | -- | -- | NC | **Not Connected.** |

## Function Description

- Reset Output

The reset output is typically connected to the reset input of a microprocessor (µP). A µP's reset input starts or restarts the µP in a known state. The PT7M7443~7452 µP supervisory circuits provide the reset logic to prevent code-execution errors during power-up, power-down and brownout conditions (see Figure 8 Typical Operating Circuit).

/RESET changes from high to low whenever the monitored voltages (RSTIN or $V_{DD}$) drop below the reset threshold voltages. Once $V_{RSTIN}$ and $V_{DD}$ exceed their respective reset threshold voltages, /RESET remains low for the reset timeout period and than goes high. /RESET is one-shot pulsed whenever selected manual reset inputs are asserted. /RESET stays asserted for the normal reset timeout period (140ms).

/RESET is guaranteed to be in the proper output logic state for $V_{DD}$ inputs ≥ 1V.

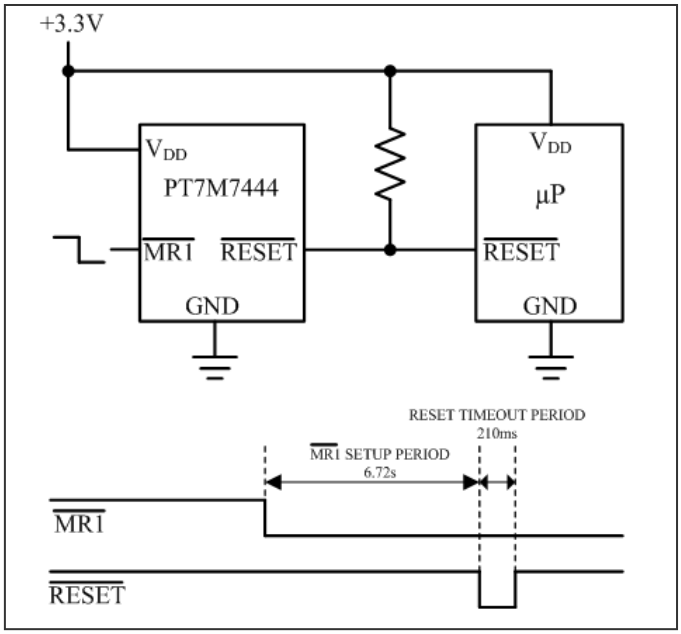



**Figure 1 Typical Operating Circuit**

- Manual Reset Input Options

Unlike typical manual reset functions associated with supervisors, each device in the PT7M7443~ 7452 family includes at lease one manual reset input, which must be held logic-low for an extended setup period (6.72 typ) before the /RESET output asserts. When valid manual reset input conditions/setup periods are met, the /RESET output is one-shot pulse asserted low for a fixed reset timeout period (140ms min). Existing front-panel pushbutton switches (i.e., power on/off, channel up/down, or mode select) can be used to drive the manual reset inputs. The extended manual reset setup period prevents nuisance system resets during normal front-panel usage or resulting from inadvertent short-term pushbutton closure.

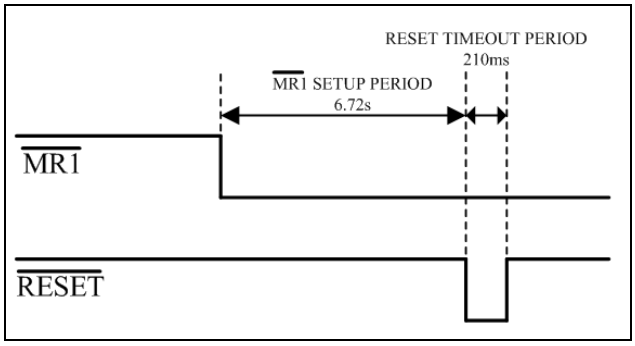



**Figure 2 PT7M7443/7444 Manual Reset Timing**

PT7M7443/7444, PT7M7447/7448, and PT7M7451/7452 include a single manual reset input with extended setup period (/MR1). The PT7M7445/7446 and PT7M7449/7450 include two manual reset inputs (/MR1 and /MR2) with extended setup periods. For dual /MR1, /MR2 devices, both inputs must be held low simultaneously for the extended setup period (6.72s typ) before the reset output is pulse asserted. The dual extended setup provides greater protection from nuisance resets. (For example, the user or service technician is informed to simultaneously push both the on/off button and the channel-select button for 6.72s to reset the system.)

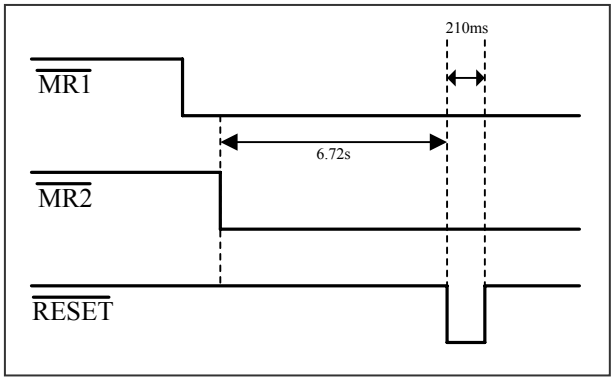



**Figure 3 PT7M7445/7446/7449/7450 Manual Reset Timing Diagram**

The PT7M7443~7452 /RESET output is pulse asserted once for the reset timeout period after each valid manual reset input condition. At least one manual reset input must be released (go high) and then be driven low for the extended setup period before /RESET asserts again. Internal timing circuitry debounces low-to-high manual reset logic transitions, so no external circuitry is required. Figure 9 illustrates the single manual reset function of the PT7M443/7444 single-voltage monitors, and Figure 10 represents the dual manual reset function of the PT7M7445/7446 and PT7M7449/7450.

The PT7M7447/7448 and PT7M7451/7452 include both an extended setup period and immediate setup period manual reset inputs. A low-to-high MR2 rising edge transition immediately pulse asserts the /RESET output for the reset timeout period (140ms min). If the PT7M7447/7448 and PT7M7451/7452 MR2 input senses another rising edge before the end of the 140ms timeout period (Figure 11), the internal timer clears and begins counting again. If no rising edges are detected within the 210ms timeout period, /RESET deasserts. The high-to-low transition on MR2 input is internally debounced for 210ms to ensure that there are no false /RESET assertions when MR2 is driven from high to low (Figure 12). The MR2 input can be used for system test purposes or smart-card-detect applications (see *Applications Information* section).

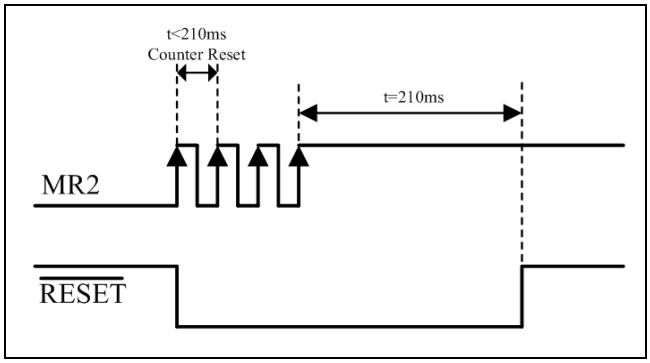



**Figure 4 PT7M7447/7448/7451/7452 MR2 Assertion Debouncing Timing Diagram**

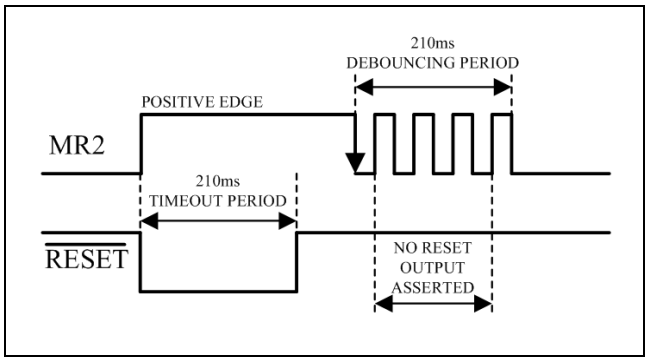



**Figure 5 PT7M7447/7448/7451/7452 MR2 Deassertion Debouncing Timing Diagram**

## Application Information

- **Adjustable Input Voltage (RSTIN)**

The PT7M7449~7452 monitor the voltage on RSTIN using an adjustable reset threshold set with an external resistor voltage-divider (see Figure 14). Use the following formula to calculate the externally monitored voltage ($V_{MON-TH}$):

$$V_{MON-TH} = V_{TH-RSTIN} \times (R1 + R2)/R2$$

Where $V_{MON-TH}$ is the desired reset threshold voltage and $V_{TH-RSTIN}$ is the reset input threshold (0.63V). Resistors R1 and R2 can have very high values to minimize current consumption because of low leakage currents. Set R2 to some conveniently high value (250kΩ, for example), and calculate R1 based on the desired reset threshold voltage, using the following formula:

$$R1 = R2 \times (V_{MON-TH} / V_{TH-RSTIN} - 1)\Omega$$

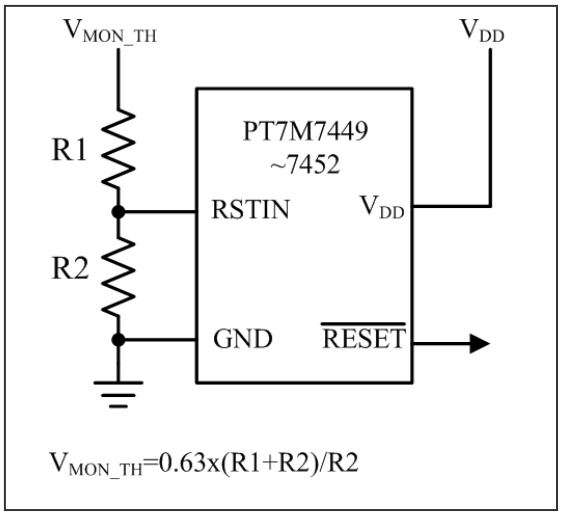



**Figure 6 PT7M7449~7452 Calculating the Monitored Threshold Voltages**

- **Interrupt Before Reset**

To minimize data loss and speed system recovery, many applications interrupt the processor or reset only portions of the system before processor hard reset is asserted. The extended setup time of the PT7M7443~7452 manual reset inputs allows the same pushbutton (connected to both the processor interrupt and the extended /MR1 input, as shown in Figure 15) to control both the interrupt and hard reset functions. If the pushbutton is closed for less than 6.72s, the processor is only interrupted. If the system still does not respond properly, the pushbutton (or two buttons for the dual manual reset) can be closed for the full extended setup period to hard reset the processor. If desired, connect an LED to the /RESET output to blink off (or on) for the reset timeout to signify when the pushbutton is closed long enough for a hard reset) the same LED might be used as the front-panel power-on display).

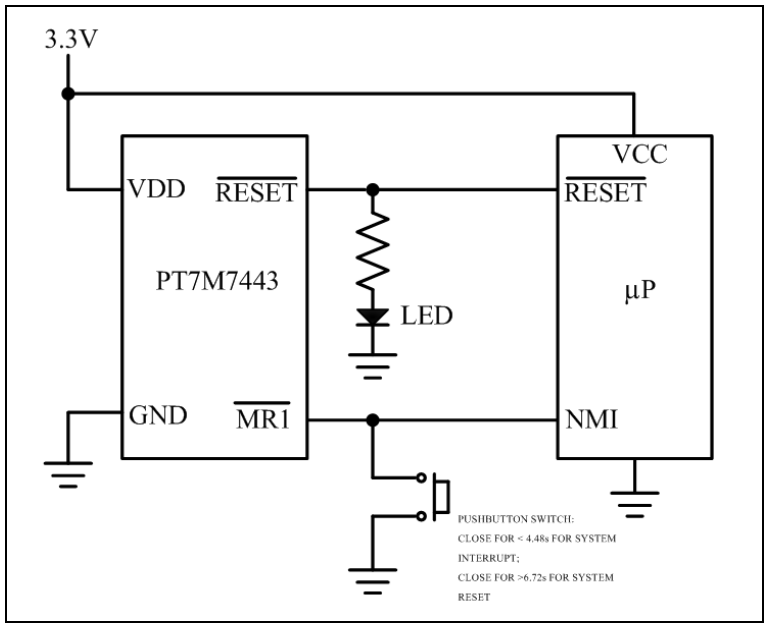



**Figure 7 Interrupt Before Reset Application Circuit**

- **Smart Card Insertion/Removal**

The PT7M7447/7448/7451/7452 dual manual resets are useful in applications in which both an extended and immediate setup periods are needed. Figure 16 illustrates the insertion and removal of a smart card. /MR1 monitors a front-panel pushbutton. When closed for 6.72s, /RESET one-shot pulses low for 140ms min. Because /MR1 is internally pulled to $V_{DD}$ through a 50kΩ resistor, the front-panel switch can be connected to a microprocessor for general-purpose I/O control. MR2 monitors a switch to detect when a smart card is inserted. When the switch is closed high (card inserted), /RESET one-shot pulses low for 140ms. MR2 is internally debounced for 210ms to prevent false resets when the smart card is removed.

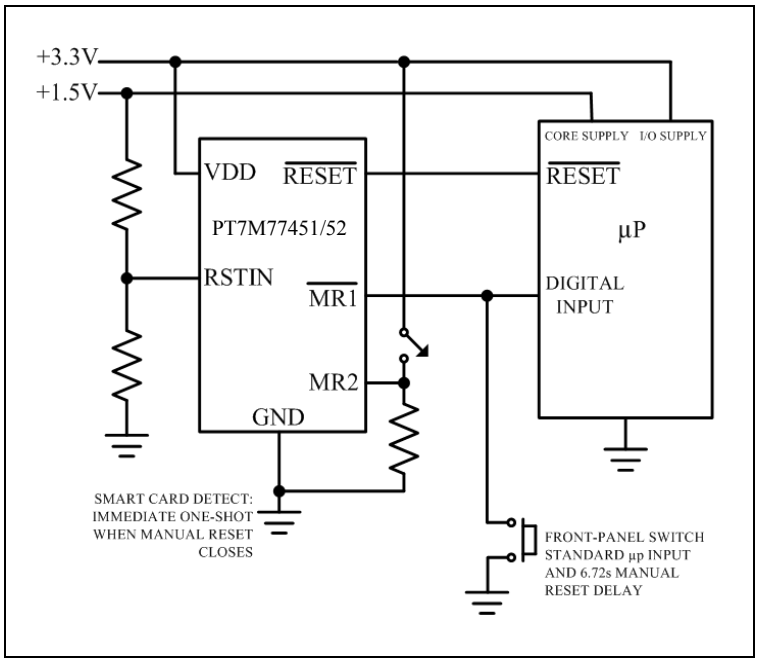



**Figure 8 PT7M7451/7452 Smart Card Detection Application Circuit**

## Maximum Ratings

Storage Temperature .....-65°C to +150°C
Ambient Temperature with Power Applied..... -55°C to +100°C
Supply Voltage to Ground Potential (Vcc to GND) .....-0.3V to +7.0V
DC Input Voltage (All inputs except Vcc and GND).....-0.3V to $V_{CC}$+0.3V
DC Output Current (All outputs) .....20mA
Power Dissipation ..... 320mW
(Depend on package)

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC Electrical Characteristics

($V_{DD}$ =1.0 to 5.5V, $T_A$= -40~85℃, unless otherwise specified. Typical values are at $T_A$ = +25℃) (Note 1)

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Voltage Range | $V_{DD}$ | $T_A$= -40~85℃ | | 1.0 | - | 5.5 | V |
| $V_{DD}$ Supply Current | $I_{DD}$ | $V_{DD}$=5.5V, no load | | - | 4 | 8 | uA |
| | | $V_{DD}$=3.6V, no load | | - | 3 | 6 | |
| $V_{DD}$ Reset Threshold | $V_{TH}$ | L | $T_A$=25℃ | 4.560 | 4.630 | 4.699 | V |
| | | | $T_A$=-40℃~85℃ | 4.500 | | 4.750 | |
| | | M | $T_A$=25℃ | 4.314 | 4.380 | 4.446 | |
| | | | $T_A$=-40℃~85℃ | 4.250 | | 4.500 | |
| | | T | $T_A$=25℃ | 3.034 | 3.080 | 3.126 | |
| | | | $T_A$=-40℃~85℃ | 3.000 | | 3.150 | |
| | | S | $T_A$=25℃ | 2.886 | 2.930 | 2.974 | |
| | | | $T_A$=-40℃~85℃ | 2.850 | | 3.000 | |
| | | R | $T_A$=25℃ | 2.590 | 2.630 | 2.669 | |
| | | | $T_A$=-40℃~85℃ | 2.550 | | 2.700 | |
| | | Z | $T_A$=25℃ | 2.285 | 2.320 | 2.355 | |
| | | | $T_A$=-40℃~85℃ | 2.250 | | 2.380 | |
| | | Y | $T_A$=25℃ | 2.157 | 2.190 | 2.223 | |
| | | | $T_A$=-40℃~85℃ | 2.120 | | 2.250 | |
| | | W | $T_A$=25℃ | 1.645 | 1.670 | 1.695 | |
| | | | $T_A$=-40℃~85℃ | 1.620 | | 1.710 | |
| | | V | $T_A$=25℃ | 1.556 | 1.580 | 1.604 | |
| | | | $T_A$=-40℃~85℃ | 1.520 | | 1.620 | |
| Reset Threshold Tempco | - | - | | - | 60 | - | ppm/℃ |
| Reset Threshold Hysteresis | - | - | | - | 2×$V_{TH}$ | - | mV |
| RSTIN Threshold | $V_{TH-RSTIN}$ | PT7M7449~7452 | $T_A$=25℃ | 0.620 | 0.630 | 0.640 | V |
| | | | $T_A$=-40℃~85℃ | 0.610 | | 0.650 | |
| RSTIN Threshold Hysteresis | $V_{HYST}$ | PT7M7449~7452 | | - | 2.5 | - | mV |
| RSTIN Input Current | $I_{RSTIN}$ | PT7M7449~7452 | | -25 | - | +25 | nA |
| RSTIN to Reset Output Delay | - | PT7M7449~7452, $V_{RSTIN}$ falling at 1mV/us | | - | 15 | - | us |
| Reset Timeout Period | $t_{RP}$ | - | | 140 | 210 | 280 | ms |

-- To be Continued --

-- Continued --

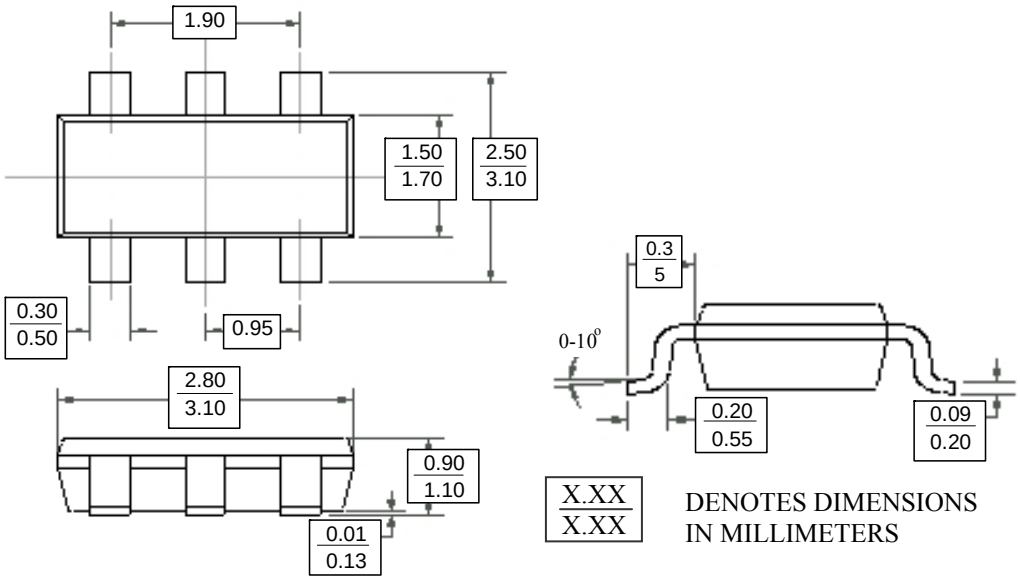
($V_{DD}$=1.0 to 5.5V, $T_A$= -40~85℃, unless otherwise specified. Typical values are at $T_A$ = +25℃) (Note 1)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ to /RESET Output Delay | $t_{RD}$ | $V_{DD}$ falling at 1mV/us | - | 20 | - | us |
| /MR1 Minimum Setup Period Pulse Width | $t_{MR}$ | - | 4.48 | 6.72 | 8.96 | s |
| /MR1+/MR2 Minimum Setup Period Pulse Width | - | PT7M7445/7446/7449/7450 | 4.48 | 6.72 | 8.96 | s |
| MR2 Minimum Setup Period Pulse Width | - | PT7M7447/7448/7451/7452 | 1 | - | - | us |
| MR2 Glitch Rejection | - | PT7M7447/7448/7451/7452 | - | 100 | - | ns |
| MR2 to /RESET Delay | - | PT7M7447/7448/7451/7452 | - | 200 | - | ns |
| Manual Reset Timeout Period | $t_{MRP}$ | - | 140 | 210 | 280 | ms |
| /MR1 to $V_{DD}$ Pull-up Impedance | - | - | 25 | 50 | 75 | kΩ |
| /MR2 to $V_{DD}$ Pull-up Impedance | - | PT7M7445/7446/7449/7450 | 25 | 50 | 75 | kΩ |
| /RESET Output Low (Open-Drain or Push-Pull) | $V_{OL}$ | $V_{DD} \geq 1.00V$, $I_{SINK}$=50uA, /RESET asserted | - | - | 0.3 | V |
| | | $V_{DD} \geq 1.20V$, $I_{SINK}$=100uA, /RESET asserted | - | - | 0.3 | |
| | | $V_{DD} \geq 2.55V$, $I_{SINK}$=1.2mA, /RESET asserted | - | - | 0.3 | |
| | | $V_{DD} \geq 4.25V$, $I_{SINK}$=3.2mA, /RESET asserted | - | - | 0.4 | |
| /RESET Output High (Push-Pull) | $V_{OH}$ | $V_{DD} \geq 1.80V$, $I_{SOURCE}$=200uA, /RESET deasserted | $0.8 \times V_{DD}$ | - | - | V |
| | | $V_{DD} \geq 3.15V$, $I_{SOURCE}$=500uA, /RESET deasserted | $0.8 \times V_{DD}$ | - | - | |
| | | $V_{DD} \geq 4.75V$, $I_{SOURCE}$=800uA, /RESET deasserted | $0.8 \times V_{DD}$ | - | - | |
| /RESET Open-Drain Leakage Current | $I_{LKG}$ | /RESET deasserted | - | - | 1 | uA |
| /MR1, /MR2, MR2 Input Low Voltage | $V_{IL}$ | - | - | - | $0.3 \times V_{DD}$ | V |
| /MR1, /MR2, MR2 Input High Voltage | $V_{IH}$ | - | $0.7 \times V_{DD}$ | - | - | V |

**Note 1:** Devices production tested at +25℃. Overtemperature limits are guaranteed by design.

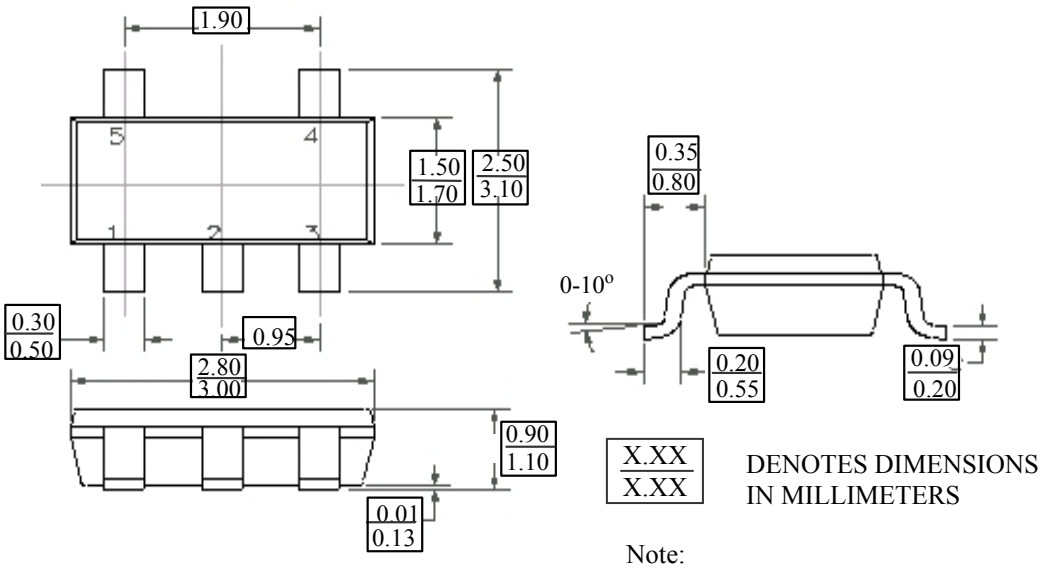
# Mechanical Information

**TAE (Lead free and Green SOT23-6)**



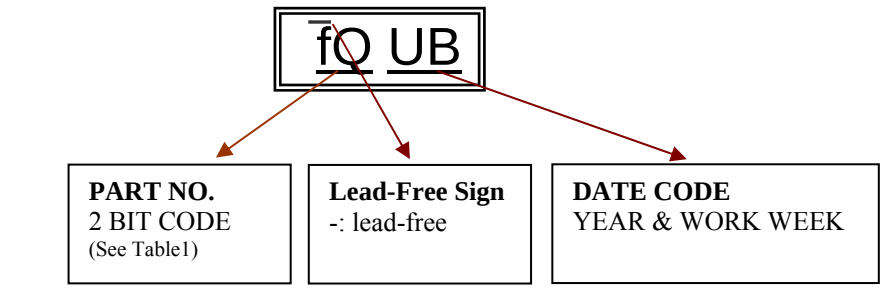

Note:
1) Controlling dimensions in millimeters.
2) Ref: JEDEC M0-178AB

**TAE (Lead free and Green SOT23-5)**




Note:
3) Controlling dimensions in millimeters.
4) Ref: JEDEC M0-178AA

## SOT-23 Package Top Marking Instruction




Sample: fQUB → PART NO.: PT7M74
DATE CODE: YEAR 2007 WW28
Lead –free package

**Table 3**

| No. | Part No. | Code | No. | Part No. | Code | No. | Part No. | Code |
|---|---|---|---|---|---|---|---|---|
| *1* | PT7M7443L | fQ | *31* | PT7M7446S | iT | *61* | PT7M7449Y | iH |
| *2* | PT7M7443M | fT | *32* | PT7M7446R | iV | *62* | PT7M7449W | iJ |
| *3* | PT7M7443T | fW | *33* | PT7M7446Z | iX | *63* | PT7M7449V | iL |
| *4* | PT7M7443S | fZ | *34* | PT7M7446Y | iZ | *64* | PT7M7450L | iN |
| *5* | PT7M7443R | gC | *35* | PT7M7446W | jB | *65* | PT7M7450M | iQ |
| *6* | PT7M7443Z | gF | *36* | PT7M7446V | jD | *66* | PT7M7450T | iS |
| *7* | PT7M7443Y | gI | *37* | PT7M7447L | fR | *67* | PT7M7450S | iU |
| *8* | PT7M7443W | gL | *38* | PT7M7447M | fU | *68* | PT7M7450R | iW |
| *9* | PT7M7443V | gO | *39* | PT7M7447T | fX | *69* | PT7M7450Z | iY |
| *10* | PT7M7444L | gS | *40* | PT7M7447S | gA | *70* | PT7M7450Y | jA |
| *11* | PT7M7444M | gV | *41* | PT7M7447R | gD | *71* | PT7M7450W | jC |
| *12* | PT7M7444T | gY | *42* | PT7M7447Z | gG | *72* | PT7M7450V | jE |
| *13* | PT7M7444S | hB | *43* | PT7M7447Y | gJ | *73* | PT7M7451L | fS |
| *14* | PT7M7444R | hE | *44* | PT7M7447W | gM | *74* | PT7M7451M | fV |
| *15* | PT7M7444Z | hH | *45* | PT7M7447V | gQ | *75* | PT7M7451T | fY |
| *16* | PT7M7444Y | hK | *46* | PT7M7448L | gT | *76* | PT7M7451S | gB |
| *17* | PT7M7444W | hN | *47* | PT7M7448M | gW | *77* | PT7M7451R | gE |
| *18* | PT7M7444V | hR | *48* | PT7M7448T | gZ | *78* | PT7M7451Z | gH |
| *19* | PT7M7445L | hU | *49* | PT7M7448S | hC | *79* | PT7M7451Y | gK |
| *20* | PT7M7445M | hW | *50* | PT7M7448R | hF | *80* | PT7M7451W | gN |
| *21* | PT7M7445T | hY | *51* | PT7M7448Z | hI | *81* | PT7M7451V | gR |
| *22* | PT7M7445S | iA | *52* | PT7M7448Y | hL | *82* | PT7M7452L | gU |
| *23* | PT7M7445R | iC | *53* | PT7M7448W | hO | *83* | PT7M7452M | gX |
| *24* | PT7M7445Z | iE | *54* | PT7M7448V | hS | *84* | PT7M7452T | hA |
| *25* | PT7M7445Y | iG | *55* | PT7M7449L | hV | *85* | PT7M7452S | hD |
| *26* | PT7M7445W | iI | *56* | PT7M7449M | hX | *86* | PT7M7452R | hG |
| *27* | PT7M7445V | iK | *57* | PT7M7449T | hZ | *87* | PT7M7452Z | hJ |
| *28* | PT7M7446L | iM | *58* | PT7M7449S | iB | *88* | PT7M7452Y | hM |
| *29* | PT7M7446M | iO | *59* | PT7M7449R | iD | *89* | PT7M7452W | hQ |
| *30* | PT7M7446T | iR | *60* | PT7M7449Z | iF | *90* | PT7M7452V | hT |

## Notes

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