

# Kinetis KL3x – General-Purpose Ultra-Low-Power MCUs

Up to 256 KB Flash and 32 KB SRAM

## 1. Kinetis L family introduction

Kinetis L series microcontrollers (MCUs) combine the exceptional low-power performance with energy efficiency and ease of use of the new ARM® Cortex®-M0+ processor with the performance, peripheral sets, enablement, and scalability of the Kinetis 32-bit MCU portfolio.

The Kinetis ultra-low-power L series frees power-critical designs from 8- and 16-bit MCU limitations by combining excellent dynamic and stop currents with superior processing performance, a broad selection of on-chip Flash memory densities, and extensive analog, connectivity, and HMI peripheral options.

Kinetis ultra-low-power L series MCUs are also hardware- and software-compatible with the ARM Cortex-M4-based Kinetis K series, providing a scalable migration path for higher performance, memory, and feature integration.

## Contents

1. Kinetis L family introduction .....	1
2. Kinetis KL3x subfamily overview.....	2
3. Kinetis KL3x family key features.....	2
4. Kinetis KL3x family feature summary .....	3
5. Kinetis KL3x family block diagram .....	4
6. KL3x family common features .....	4
7. Kinetis KL3x family differences .....	5
8. Comprehensive enablement solutions .....	6
8.1. Kinetis Software Development Kit (SDK).....	6
8.2. Processor Expert .....	6
8.3. Integrated development environments (IDE) .....	6
8.4. Online enablement with ARM mbed™ development platform .....	7
8.5. Freescale MQX™ Lite RTOS .....	7
8.6. Boot-loader .....	7
8.7. Development hardware .....	7
9. Part identification .....	7
9.1. Description .....	7
9.2. Format .....	8
9.3. Fields.....	8
10. Orderable part numbers .....	8

## 2. Kinetis KL3x subfamily overview

The Kinetis KL3x ultra low power MCU family adds a segment LCD controller in addition to the Kinetis KL1x series. The Kinetis KL3x MCU family is also compatible with the Kinetis K30 MCU family (based on the ARM® Cortex®-M4 processor), and with all other Kinetis KL1x, KL2x, and KL4x series MCUs, providing a migration path to lower and higher performance and feature integration.

- KL33 – New member of KL3x, with up to 256KB flash and 32KB SRAM, featuring ROM boot loader, FlexIO, ISO7816 and, 16-bit ADC, 12-bit DAC, and high accuracy internal VREF.
- KL34 – General purpose MCU with segment LCD, featuring market leading ultra low power to provide developers an appropriate entry-level 32-bit solution.
- KL36 – Expansion from the KL34 with up to 256 KB Flash and 32 KB SRAM, with the addition of 16-bit ADC, 12-bit DAC, I2S, and TSI

## 3. Kinetis KL3x family key features

- Ultra-low-power 48 MHz devices supported with base line functions, up to 256 KB of Flash, and 32 KB of RAM.
- The asynchronous DMA allows for energy-saving peripherals; for example, ADC, UART, and Timer / PWM, to trigger asynchronous DMA request in the STOP / VLPS modes to perform DMA transfer and return to current power mode with no CPU intervention.
- Segment LCD controller is available under all power mode (except VLLS0).
- The LPUART supports asynchronous transmit and receive operations to the bus clock, supporting communication down to the STOP / VLPS modes. Configurable receiver baud rate oversampling ratio from 4× to 32×, allowing for higher baud rates with lower clock sources.
- The SPI supports slave mode address match wakeup function and first message capture down to the STOP / VLPS modes.
- The I<sup>2</sup>C supports multiple address match wakeup function down to the STOP / VLPS modes.
- The FlexIO is capable of emulating multiple serial interfaces, for example, UART, SPI, I<sup>2</sup>C, IrDA, and is fully-functional under the STOP / VLPS modes.
- The LPTPM supports 16-bit timer input capture, output compare, and PWM functions, down to the STOP / VLPS modes.
- The LPTMR supports 16-bit timer and pulse counter functions in all power modes.
- The RTC supports 32-bit second counter with second interrupt and programmable alarm in all power modes with included temperature and voltage compensation.
- The ADC supports single conversions in multiple result registers down to the STOP / VLPS modes with hardware averaging and automatic compare modes.
- The CMP supports threshold crossing detection in all power modes (except VLLS0) along with a triggered compare mode for lower average power compares.

- The DAC and VREF support static reference in all power modes (except VLLS0).
- The TSI supports wake-on capacitive touch on single channel in all power modes.
- The LLWU supports eight wakeup pins, RESET and NMI wakeup pins, and energy-saving peripherals in the LLS and VLLSx modes.
- Outstanding low-power operation with core mark currents down to 100  $\mu\text{A}$  / MHz, state retention stop mode down to 1.83  $\mu\text{A}$ , with 7.5  $\mu\text{S}$  wakeup time, and lowest power mode down to 95 nA.
- Highly reliable, fast-access Flash memory with four levels of protection for code security / protection.
- Faster time to market with comprehensive enablement solutions, including SDK (drivers, libraries, stacks), IDE, boot-loader, RTOS, online community, and more.

## 4. Kinetis KL3x family feature summary

**Table 1. Family feature summary**

Sub-Family	KL33	KL34	KL36
CPU Frequency	48MHz	48MHz	48MHz
Flash Memory	32-256KB	64KB	32-256KB
SRAM	4-32KB	8KB	4-32KB
ROM Bootloader	Yes	-	-
Segment LCD	40x8/42x6/44x4 - 20x8/22x6/24x4	51x8/55x4 - 28x8/32x4	51x8/55x4 - 28x8/32x4
Analog	16bit ADC, 12bitDAC, CMP, VREF	12bit ADC, CMP	16bit ADC, 12bit DAC, CMP
Connectivity	UART w/ ISO7816, LPUART,SPI, I2C, I2S, FlexIO	UART,LPUART, SPI, I2C	UART,LPUART, SPI, I2C I2S
Package Options	48QFN, 64LQFP, 64MAPBGA, 80LQFP	64LQFP, 100LQFP	64LQFP, 64MAPBGA, 100LQFP, 121MAPBGA

## 5. Kinetis KL3x family block diagram

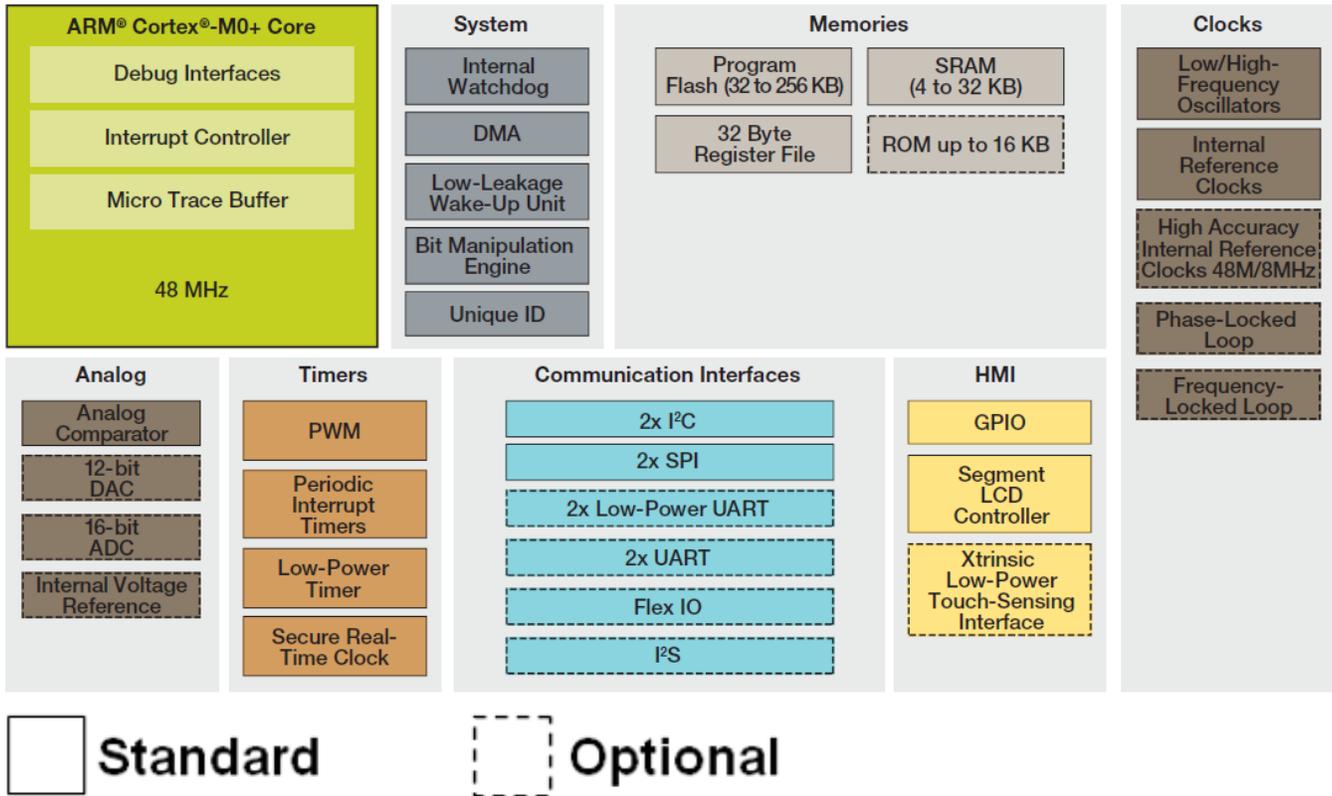


Figure 1. Kinetis KL3x family block diagram

## 6. KL3x family common features

The following features are present on all KL3x MCUs:

- 48 MHz Cortex-CM0+
- 2-pin serial wire debug (SWD), micro trace buffer (MTB)
- 4-channel DMA controller
- Integrated bit manipulation engine (BME)
- 64-Byte cache and 32-Byte register file
- 1 × 6-channel and 2 × 2-channel LPTPM
- Low- and high-frequency OSC
- RTC (32 KHz OSC)
- 1 × low-power timer, 1 × 2-channel PIT
- High-speed analog comparator containing a 6-bit DAC for programmable reference input

- Power management controller (PMC) with nine power modes
- Non-maskable interrupt (NMI)
- Software and COP watchdog
- 80-bit unique identification number per chip
- Voltage range 1.71 V – 3.6 V
- Temperature range (T<sub>A</sub>) -40°C – 105°C

## 7. Kinetis KL3x family differences

Table 2. Family differences

Subfamily		KL33	KL34	KL36
CPU frequency		48MHz	48MHz	48MHz
Memory	Flash / SRAM Size	32KB/4KB - 256KB/32KB	32KB/4KB - 64KB/8KB	32KB/4KB - 256KB/32KB
	Boot ROM	Yes	-	-
Communication Interface	LPUART	2	1	1
	UART	-	2	2
	UART w/ ISO7816	1	-	-
	SPI	2	2	2
	I2C	2 <sup>1</sup>	2	2
	I2S	Optional <sup>2</sup>	-	1
	FlexIO	Yes	-	-
Analog Modules	ADC	16-bit	12-bit	16-bit
	ADC channels (SE / DE)	17/3 - 20/4	20/0	20/4
	DAC	12-bit	-	12-bit
	VREF	Yes	-	-
Other Modules	CRC	Optional <sup>3</sup>	-	-
	Segment LCD	40x8/42x6/44x4 - 20x8/22x6/24x4	51x8/55x4 - 28x8/32x4	51x8/55x4 - 28x8/32x4
	TSI	-	-	16ch
	Total GPIOs	40-70	54-84	54-84

	MCG	High Accuracy 48M IRC, 8M/2M IRC	4M/32KHz IRC PLL/FLL	4M/32KHz IRC PLL/FLL
<b>Package Options</b>		48QFN, 64LQFP, 64MAPBGA, 80LQFP	64LQFP, 100LQFP	64LQFP, 64MAPBGA, 100LQFP, 121MAPBGA

<sup>1</sup>Support 1M bps

<sup>2</sup>I2S is only available in 128KB and 256KB flash KL33

<sup>3</sup>CRC is only available in 32KB and 64KB flash KL33

## 8. Comprehensive enablement solutions

### 8.1. Kinetis Software Development Kit (SDK)

- Extensive suite of robust peripheral drivers, stacks, and middleware.
- Includes software examples demonstrating the usage of HAL, peripheral drivers, middleware, and RTOSes.
- Operating system abstraction (OSA) for Freescale MQX™ Lite RTOS, FreeRTOS, and Micrium uC / OS kernels and bare-metal (no RTOS) applications.

### 8.2. Processor Expert

- Free software generation tool for device drivers / start-up code
- Seven steps from project creation to debug – dramatically reduces development time
- Available within Kinetis Design Studio or as a standalone plug-in for IAR/Keil/GNU IDEs

### 8.3. Integrated development environments (IDE)

- Freescale Kinetis Design Studio IDE
  - No-cost integrated development environment (IDE) for Kinetis MCUs
  - Eclipse and GCC-based IDE for C / C++ editing, compiling, and debugging
- IAR Embedded Workbench® [iar.com/kinetis](http://iar.com/kinetis)
- ARM Keil® Microcontroller Development Kit [keil.com/freescale](http://keil.com/freescale)
- Atollic® TrueSTUDIO® [atollic.com/index.php/partnerfreescale](http://atollic.com/index.php/partnerfreescale)
- Green Hills Software MULTI [ghs.com/products/kinetis.html](http://ghs.com/products/kinetis.html)
- Broad ARM ecosystem support through Freescale Connect partners

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## 8.4. Online enablement with ARM mbed™ development platform

- Rapid and easy Kinetis MCU prototyping and development
- Online mbed SDK, developer community
- Free software libraries

## 8.5. Freescale MQX™ Lite RTOS

- Free, light-weight MQX kernel customised for small resource MCUs
- Packaged as a Processor Expert component
- Upwards compatible with MQX RTOS

## 8.6. Boot-loader

- Common boot-loader for all Kinetis MCUs
- In-system Flash programming over a serial connection: erase, program, verify
- ROM- or Flash-based boot-loader with open-source software and host-side programming utilities

## 8.7. Development hardware

- Tower System modular development platform
  - Modular and Expandable
  - Rapid prototyping and evaluation
  - Cost Effective
- Freescale Freedom development platforms
  - Low cost (< \$ 15 USD)
  - Designed in an industry-standard compact form factor
  - Integrated open-standard serial and debug interface (OpenSDA)
  - Compatible with a rich-set of third-party expansion boards

# 9. Part identification

## 9.1. Description

The chip part numbers have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 9.2. Format

The device part numbers have the following format: Q KL## A FFF T PP CC (N)

## 9.3. Fields

The following table lists the possible values for each field in the part number (not all combinations are valid).

**Table 3. Part number field descriptions**

Field	Description	Values
Q	Qualification status	M = Fully-qualified, general market flow P = Prequalification
KL##	Kinetis family	KL33 KL34 KL36
A	Key attribute	Z = Cortex-M0+
FFF	Program Flash memory size	32 = 32 KB 64 = 64 KB 128 = 128 KB 256 = 256 KB
R	Silicon revision	(Blank) = Main A = Revision after main
T	Temperature range	V = -40°C – 105°C
PP	Package identifier	FM = 32QFN (5 mm × 5 mm × 0.65 mm, Pitch 0.5mm) FT = 48QFN (7 mm × 7 mm × 0.65mm, Pitch 0.5mm) LH = 64LQFP (10 mm × 10 mm × 1.4mm, Pitch 0.5mm) MP = 64MAPBGA (5 mm × 5 mm × 1.5mm, Pitch 0.5mm) LK = 80LQFP (12 mm × 12 mm × 1.6mm, Pitch 0.5mm) LL = 100LQFP (14 mm × 14 mm × 1.7mm, Pitch 0.5mm) MC = 121MAPBGA (8 mm × 8 mm × 1.5mm, Pitch 0.65mm)
CC	Maximum CPU frequency (MHz)	4 = 48 MHz
N	Packaging type	R = Tape and reel (Blank) = Trays

## 10. Orderable part numbers

**Table 4. Ordering information**

Product	Memory		Package		HMI and ADC Channel			
	Flash (KB)	SRAM (KB)	Pin Count	Package	GPIOs	GPIOs (INT/HD) <sup>1</sup>	LCD Segments	ADC channels (SE/DP)
MC Part number								
MKL33Z32VFT4	32	4	48	QFN <sup>2</sup>	40	40/4	20x8/22x6/24x4	17/3

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Product	Memory		Package		HMI and ADC Channel			
	MC Part number	Flash (KB)	SRAM (KB)	Pin Count	Package	GPIOs	GPIOs (INT/HD) <sup>1</sup>	LCD Segments
MKL33Z32VLH4	32	4	64	LQFP	54	54/4	28x8/30x6/32x4	20/4
MKL33Z32VMP4	32	4	64	MAPBGA <sup>2</sup>	54	54/4	28x8/30x6/32x4	20/4
MKL33Z32VLK4	32	4	80	LQFP	70	70/4	40x8/42x6/44x4	20/4
MKL33Z64VFT4	64	8	48	QFN <sup>2</sup>	40	40/4	20x8/22x6/24x4	17/3
MKL33Z64VLH4	64	8	64	LQFP	54	54/4	28x8/30x6/32x4	20/4
MKL33Z64VMP4	64	8	64	MAPBGA <sup>2</sup>	54	54/4	28x8/30x6/32x4	20/4
MKL33Z64VLK4	64	8	80	LQFP	70	70/4	40x8/42x6/44x4	20/4
MKL33Z128VLH4	128	16	64	LQFP	54	31/6	28x8/32x4	20/4
MKL33Z128VMP4	128	16	64	MAPBGA	54	31/6	28x8/32x4	20/4
MKL33Z256VLH4	256	32	64	LQFP	54	31/6	28x8/32x4	20/4
MKL33Z256VMP4	256	32	64	MAPBGA	54	31/6	28x8/32x4	20/4
MKL34Z64VLH4	64	8	64	LQFP	54	31/4	28x8/32x4	20/0
MKL34Z64VLL4	64	8	100	LQFP	84	46/4	51x8/55x4	20/0
MKL36Z64VLH4	64	8	64	LQFP	54	31/4	28x8/32x4	20/4
MKL36Z64VLL4	64	8	100	LQFP	84	46/4	51x8/55x4	20/4
MKL36Z128VLH4	128	16	64	LQFP	54	31/4	28x8/32x4	20/4
MKL36Z128VLL4	128	16	100	LQFP	84	46/4	51x8/55x4	20/4
MKL36Z128VMC4	128	16	121	MAPBGA	84	46/4	51x8/55x4	20/4
MKL36Z256VLH4	256	32	64	LQFP	54	31/4	28x8/32x4	20/4
MKL36Z256VLL4	256	32	100	LQFP	84	46/4	51x8/55x4	20/4
MKL36Z256VMC4	256	32	121	MAPBGA	84	46/4	51x8/55x4	20/4
MKL36Z256VMP4	256	32	64	MAPBGA	54	31/4	28x8/32x4	20/4

<sup>1</sup> INT: interrupt pin numbers; HD: high drive pin numbers

<sup>2</sup> This package is included in a Package Your Way program for Kinetis MCUs. Please visit [Freescale.com/KPYW](http://Freescale.com/KPYW) for more detail.

**Table 5. Revision history**

Revision	Substantial changes
0	Initial release



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