TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (L^2−π−MOSV)

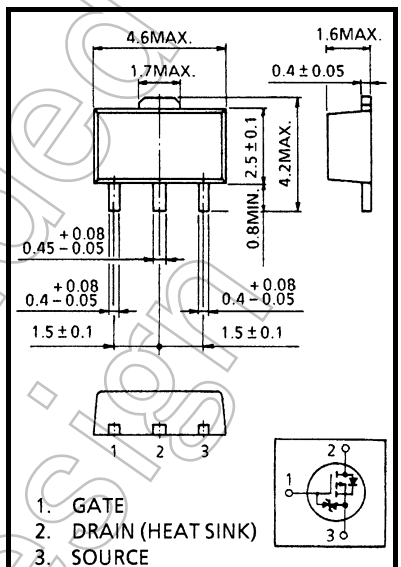
2SJ360

High Speed, High current Switching Applications

Chopper Regulator, DC−DC Converter and Motor Drive Applications

- 4-V gate drive
- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 0.55 Ω (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 0.9 S (typ.)
- Low leakage current : I_{DSS} = −100 μA (max) (V_{DS} = −60 V)
- Enhancement mode : V_{th} = −0.8 to −2.0 V (V_{DS} = −10 V, I_D = −1 mA)

Unit: mm



JEDEC	—
JEITA	SC-62
TOSHIBA	2−5K1B

Weight: 0.05 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	−60	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−60	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	−1	A
	Pulse (Note 1)	I_{DP}	−4	A
Drain power dissipation		P_D	0.5	W
Drain power dissipation (Note 2)		P_D	1.5	W
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Mounted on a ceramic substrate (25.4 mm × 25.4 mm × 0.8 mm)

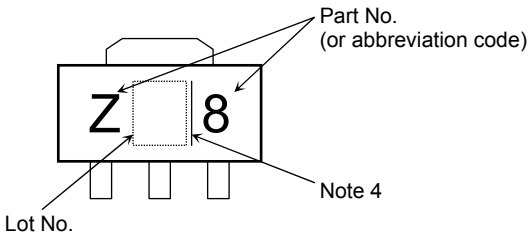
Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	250	°C / W

This transistor is an electrostatic-sensitive device. Please handle with caution.

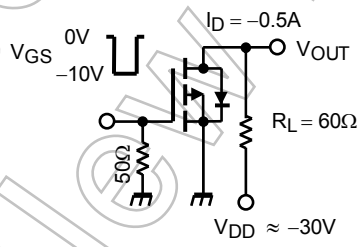
Marking



Note 4: A line to the right of a Lot No. identifies the indication of product Labels.
Without a line: [[Pb]]/INCLUDES > MCV
With a line: [[G]]/RoHS COMPATIBLE or [[G]]/RoHS [[Pb]]

Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. The RoHS is the Directive 2002/95/EC of the European Parliament and of the Council of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment.

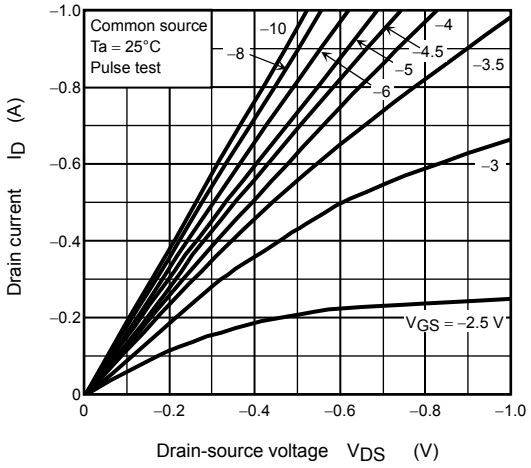
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = −60 V, V_{GS} = 0 V	—	—	−100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−60	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−0.8	—	−2.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −4 V, I_D = −0.5 A	—	0.86	1.2	Ω
			V_{GS} = −10 V, I_D = −0.5 A	—	0.55	0.73	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −0.5 A	0.5	1.0	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	155	—	pF
Reverse transfer capacitance		C_{rss}		—	22	—	
Output capacitance		C_{oss}		—	75	—	
Switching time	Rise time	t_r		—	17	—	ns
	Turn−on time	t_{on}		—	20	—	
	Fall time	t_f		—	20	—	
	Turn−off time	t_{off}		—	100	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ −48 V, V_{GS} = −10 V, I_D = −1 A	—	6.5	—	nC
Gate−source charge		Q_{gs}		—	4.5	—	
Gate−drain (“miller”) charge		Q_{gd}		—	2.0	—	

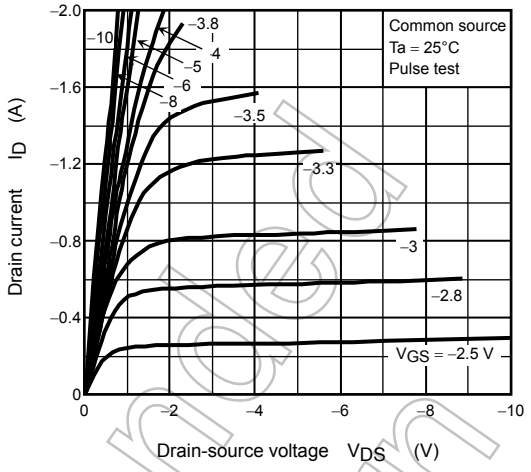
Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	−1	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	−4	A
Forward voltage (diode)	V_{DSF}	I_{DR} = −1 A, V_{GS} = 0 V	—	—	1.8	V
Reverse recovery time	t_{rr}	I_{DR} = −1 A, V_{GS} = 0 V dI_{DR} / dt = 50 A / μs	—	50	—	ns
Reverse recovery charge	Q_{rr}		—	45	—	nC

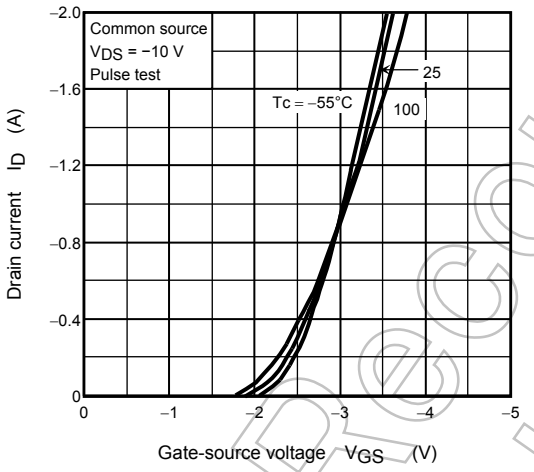
$I_D - V_{DS}$



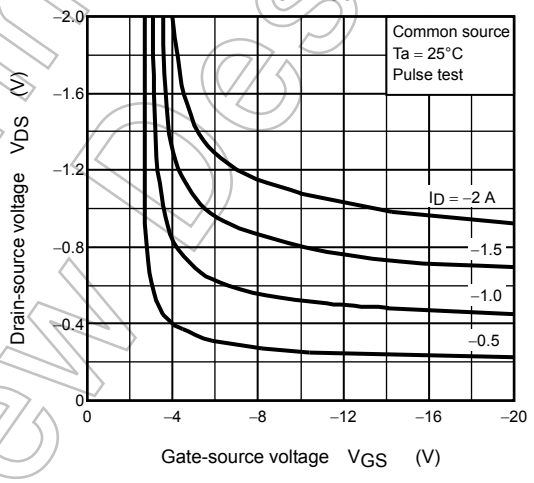
$I_D - V_{DS}$



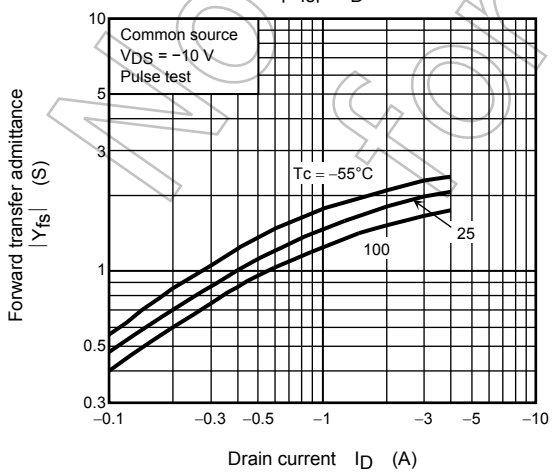
$I_D - V_{GS}$



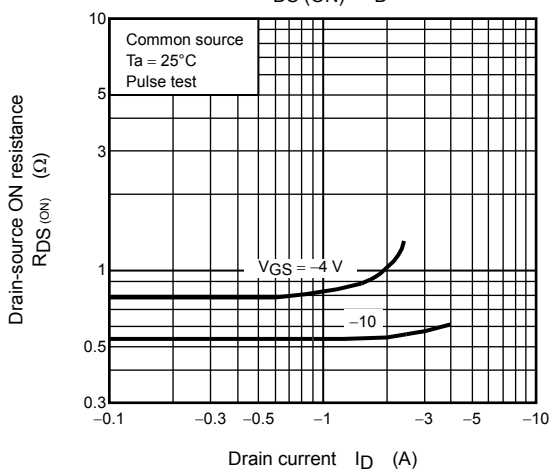
$V_{DS} - V_{GS}$



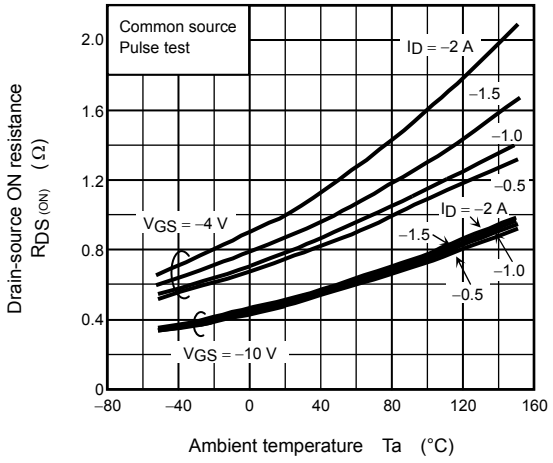
$|Y_{fs}| - I_D$



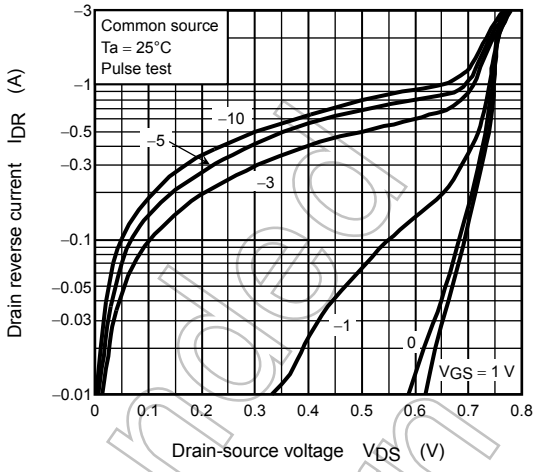
$R_{DS\ (ON)} - I_D$



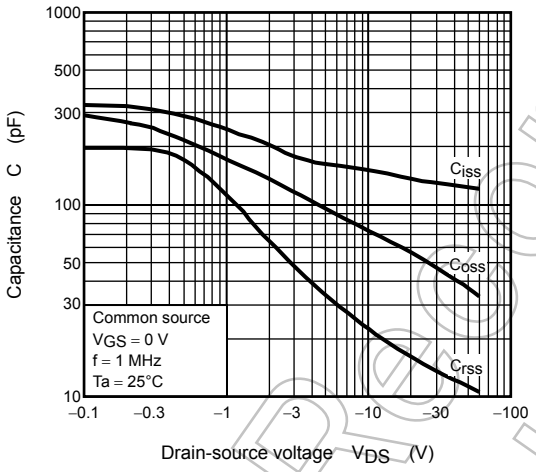
$R_{DS\ (ON)}$ – Ta



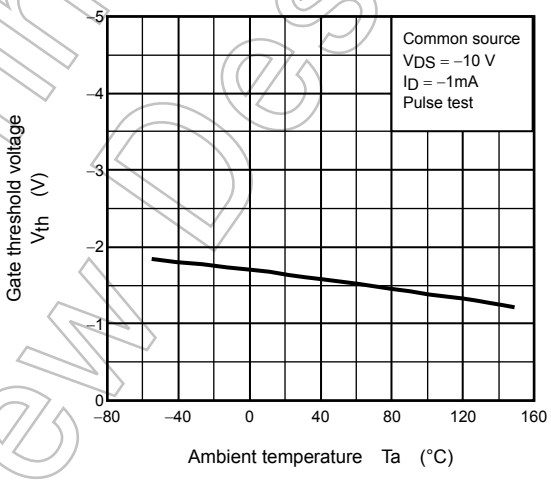
I_{DR} – V_{DS}



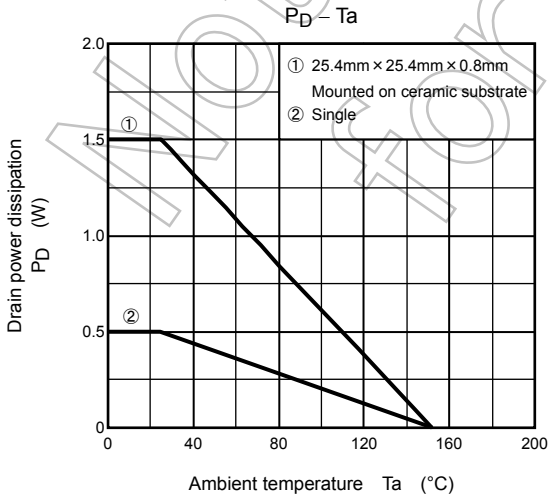
Capacitance – V_{DS}

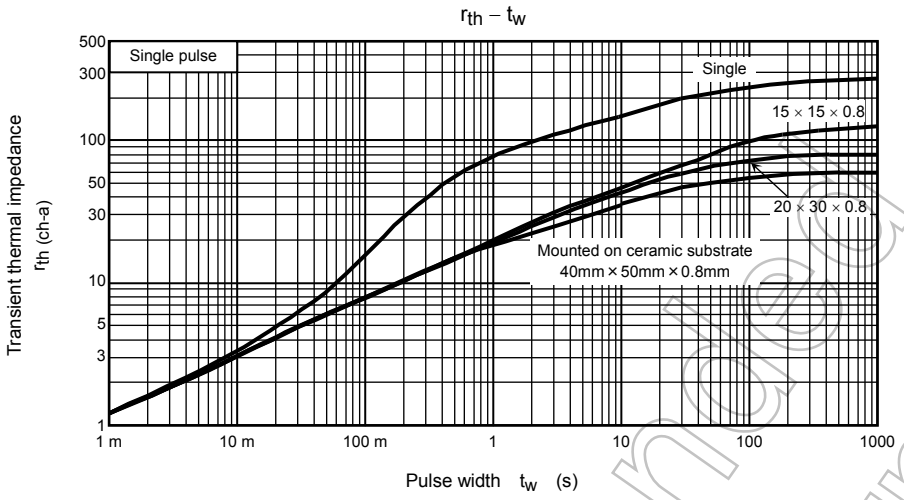


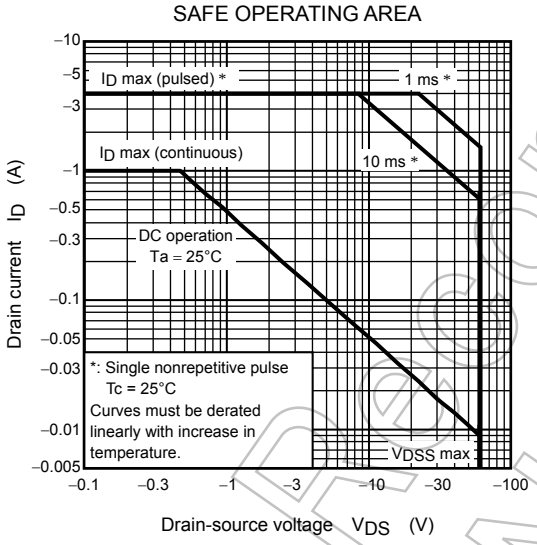
V_{th} – Ta



P_D – Ta







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