PIC18F2410/2510/4410/4510 Rev. B3 Silicon Errata

The PIC18F2410/2510/4410/4510 Rev. B3 parts you have received conform functionally to the Device Data Sheet (DS39636**D**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2410/2510/4410/4510 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2410/2510/4410/4510 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2410	0001 0001 011	0 0110
PIC18F2510	0001 0001 001	0 0110
PIC18F4410	0001 0000 111	0 0110
PIC18F4510	0001 0000 101	0 0110

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

All of the issues listed here will be addressed in future revisions of the PIC18F2410/2510/4410/4510 silicon.

1. Module: MSSP

In SPI Slave mode with slave select enabled (SSPM<3:0> = `0100`), the minimum time between the falling edge of the $\overline{SS}$ pin and first SCK edge is greater than specified in parameter 70 in Table 25-16 and Table 25-17 of the above referenced data sheet.

The updated specification is shown in bold in Table .

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

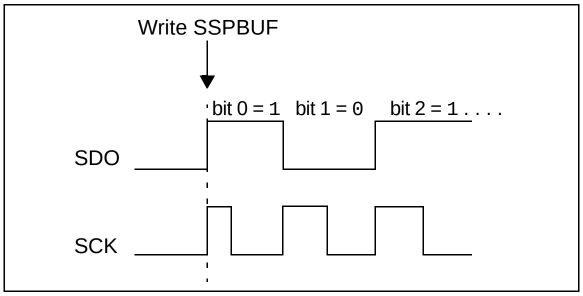
TABLE 1: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING)

Param No.	Symbol	Characteristic	Min.	Max.	Units	Conditions
70	TssL2sc, TssL2scL	$\overline{SS}$ ↓ to SCK ↓ or SCK ↑ Input	**3 TCY**	—	ns	

2. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 1 for sample code.

EXAMPLE 1: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSS SSPSTAT, BF     ;Data received?
                           ;(Xmit complete?)
     BRA   LOOP            ;No
     MOVF  SSPBUF, W       ;W = SSPBUF
     MOVWF RXDATA          ;Save in user RAM
     MOVF  TXDATA, W       ;W = TXDATA
     BCF   T2CON, TMR2ON   ;Timer2 off
     CLRF  TMR2            ;Clear Timer2
     MOVWF SSPBUF          ;Xmit New data
     BSF   T2CON, TMR2ON   ;Timer2 on
```

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

One bit has been added to the BAUDCON register and one bit has been renamed. The added bit is RXDTP and is in the location, BAUDCON<5>. The renamed bit is the TXCKP bit (BAUDCON<4>), which had been named SCKP.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits enable the TX and RX signals to be inverted (polarity reversed).

Register 17-3, on page 194, will be changed as shown on page 3.

Work around

None required.

Date Codes that pertain to this issue:

All engineering and production devices.

REGISTER 17-3: BAUDCON: BAUD RATE CONTROL REGISTER

R-0/0	R-1/1	U-0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0
ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ABDOVF:** Auto-Baud Acquisition Rollover bit
Asynchronous mode:
1 = A BRG rollover has occurred during Auto-Baud Rate Detect mode (must be cleared in software)
0 = No BRG rollover has occurred

bit 6 **RCIDL**: Receive Operation Idle Status bit
1 = Receive operation is Idle
0 = Receive operation is Active

bit 5 **RXDTP**: Receive Data Polarity Select bit
Asynchronous mode:
1 = Receive data (RX) is inverted. Idle state is a low level.
0 = No inversion of the receive data (RX). IIdle state is a high level.
Synchronous mode:
1 = Data (DT) is inverted. Idle state is a low level.
0 = No inversion of the data (DT). IIdle state is a high level.

bit 4 **TXCKP**: Transmit/Clock Polarity Select bit
Asynchronous mode:
1 = Transmit data (TX) is inverted. Idle state is a low level
0 = No inversion of the transmit data (TX). IIdle state is a high level
Synchronous mode:
1 = IIdle state for clock (CK) is a high level.
0 = IIdle state for clock (CK) is a low level

bit 3 **BRG16:** 16-bit Baud Rate Generator bit
1 = 16-bit Baud Rate Generator is used
0 = 8-bit Baud Rate Generator is used

bit 2 **Unimplemented:** Read as '0'

bit 1 **WUE:** Wake-up Enable bit
Asynchronous mode:
1 = Receiver is waiting for a falling edge. No character will be received, byte RCIF will be set. WUE will automatically clear after RCIF is set.
0 = Receiver is operating normally
Synchronous mode:
Don't care

bit 0 **ABDEN**: Auto-Baud Detect Enable bit
Asynchronous mode:
1 = Auto-Baud Detect mode is enabled (clears when auto-baud is complete)
0 = Auto-Baud Detect mode is disabled
Synchronous mode:
Don't care

4. Module: Timer1/3

When Timer1 or Timer3 is operated in Asynchronous External Input mode, unexpected interrupt flag generation may occur if an external clock edge arrives too soon following a firmware write to the TMRxH:TMRxL registers. An unexpected interrupt flag event may also occur when enabling the module or switching from Synchronous to Asynchronous mode.

Work around

This issue only applies when operating the timer in Asynchronous mode. Whenever possible, operate the timer module in Synchronous mode to avoid spurious timer interrupts.

If Asynchronous mode must be used in the application, potential strategies to mitigate the issue may include any of the following:

- Design the firmware so it does not rely on the TMRxIF flag or keep the respective interrupt disabled. The timer still counts normally and does not reset to `0x0000` when the spurious interrupt flag event is generated.
- Design the firmware so that it does not write to the TMRxH:TMRxL registers or does not periodically disable/enable the timer, or switch modes. Reading from the timer does not trigger the spurious interrupt flag events.
- If the firmware must use the timer interrupts and must write to the timer (or disable/enable, or mode switch the timer), implement code to suppress the spurious interrupt event, should it occur. This can be achieved by following the process shown in Example 2.

EXAMPLE 2: ASYNCHRONOUS TIMER MODE WORK AROUND TO AVOID SPURIOUS INTERRUPT

```
//Timer1 update procedure in asynchronous mode
//The code below uses Timer1 as example

T1CONbits.TMR1ON = 0;         //Stop timer from incrementing
PIE1bits.TMR1IE = 0;          //Temporarily disable Timer1 interrupt vectoring
TMR1H = 0x00;                 //Update timer value
TMR1L = 0x00;
T1CONbits.TMR1ON = 1;         //Turn on timer

//Now wait at least two full T1CKI periods + 2TCY before re-enabling Timer1 interrupts.
//Depending upon clock edge timing relative to TMR1H/TMR1L firmware write operation,
//a spurious TMR1IF flag event may sometimes assert. If this happens, to suppress
//the actual interrupt vectoring, the TMR1IE bit should be kept clear until
//after the "window of opportunity" (for the spurious interrupt flag event has passed).
//After the window is passed, no further spurious interrupts occur, at least
//until the next timer write (or mode switch/enable event).

while(TMR1L < 0x02);          //Wait for 2 timer increments more than the Updated Timer
                              //value (indicating more than 2 full T1CKI clock periods elapsed)
NOP();                        //Wait two more instruction cycles
NOP();
PIR1bits.TMR1IF = 0;          //Clear TMR1IF flag, in case it was spuriously set
PIE1bits.TMR1IE = 1;          //Now re-enable interrupt vectoring for timer 1
```

5. Module: 10-Bit Analog-to-Digital (A/D) Converter

When the A/D clock source is selected as 2 T_{OSC} or RC (when ADCS2:ADCS0 = `000` or `x11`), in extremely rare cases, the E_{IL} (Integral Linearity Error) and E_{DL} (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select a different A/D clock source (4 T_{OSC}, 8 T_{OSC}, 16 T_{OSC}, 32 T_{OSC}, 64 T_{OSC}) and avoid selecting the 2 T_{OSC} or RC modes.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (4/2007)

Initial revision of this document. Silicon issue 1 (MSSP), 2 (MSSP – SPI Mode) and 3 (Enhanced Universal Synchronous Receiver Transmitter – EUSART).

Rev B Document (8/2007)

Added silicon issue 4 (10-Bit A/D Converter).

Rev C Document (01/2015)

Added Module 4 (Timer1/3).

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