Errata

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10. LDS/STS when Accessing External RAM

Using an LDS instruction for reading external RAM corrupts the source register used in the LDS instruction when directly followed by NOP. An STS instruction for writing to external RAM corrupts R0 when directly followed by NOP.

Problem Fix/Workaround

Do not insert a NOP instruction directly after an LDS or STS instruction used for accessing the external SRAM.

9. STS when Accessing EEPROM

If the STS instruction is used to start an EEPROM write (EEWE in EECR), the following instruction may have an undesired result. In the case of NOP, R0 will be corrupted.

Problem Fix/Workaround

Use the OUT or SBI instruction to start an EEPROM write.

8. COM1B Settings Never Disconnects OC1B

According to the datasheet, Timer/Counter1 should be disconnected from the OC1B pin when COM1B[1:0] = “00” in non-PWM mode, and when COM1B[1:0] = “00” or “01” in PWM mode. This, however, is not the case.

For OC1A, the description in the datasheet is correct; the general digital I/O function takes over.

Problem Fix/Workaround

As OC1B is an output only pin with no general digital I/O function, the pin cannot be tri-staded. However, if there is a need to stop the pin from toggling, disable the PWM mode by setting PWM[1:0] to “00” and set the COM1A[1:0] to anything else than “01” (which is the toggle mode). Warning: As long as the timer is still running, the counter can count to a value above the maximum for that PWM mode. As an alternative, the timer can be stopped by setting CS1[2:0] in TCCR1B to “000”.

7. UART Loses Synchronization if RXD Line is Low when UART Receive is Disabled

The UART will detect an UART start bit and start reception even if the UART is not enabled. If this occurs, the first byte after re-enabling the UART will be corrupted.

Problem Fix/Workaround

Make sure that the RX line is high at start-up and when the UART is disabled. An external RS232-level converter keeps the line high during start-up.

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6. Releasing Reset Condition without Clock

If an external reset or a watchdog reset occurs while the clock is stopped and the reset is released before the clock is restarted, the internal reset will timeout after the start-up delay which is independent of the external clock. If no external clock pulses are present in the period when internal reset is active, the reset does correctly cause tristating of the I/O while the reset is held. However, if the internal reset is released before the clock starts running, the part does not clear I/O registers, nor set PC to 0x00. Here, stopping the clock refers to gating the external clock input. Power-down mode does not have this issue.

Problem Fix/Workaround

Make sure the clock is running whenever an external reset can be expected. If the Watchdog is used, never stop an external clock.

5. The SPI Can Send Wrong Byte

If the SPI is in master mode, it will restart the old transfer if new data is written on the same clock edge as the previous transfer is finished.

Problem Fix/Workaround

When writing to the SPI, first wait until it is ready; then write the byte to transmit.

4. Reset during EEPROM Write

If reset is activated during EEPROM write, the result is not what should be expected. The EEPROM write cycle completes as normal, but the address registers are reset to 0. The result is that both the address written and address 0 in the EEPROM can be corrupted.

Problem Fix/Workaround

Avoid using address 0 for storage, unless you can guarantee that you will not get a reset during EEPROM write.

3. SPI Interrupt Flag Can be Undefined after Reset

In certain cases when there are transitions on the SCK pin during reset, or the SCK pin is left unconnected, the start-up value of the SPI interrupt flag is unknown. If the flag is not reset before enabling the SPI interrupt, a pending SPI interrupt may be executed.

Problem Fix/Workaround

Clear the SPI interrupt flag before enabling the interrupt.

2. Serial Programming at Voltages below 3.0 Volts

At voltages below 3.0 volts, serial programming might fail.

Problem Fix/Workaround

Keep V_{CC} at 3.0 volts or higher during In-System Programming.

1. Skip Instruction with Interrupts

A skip instruction (SBRS, SBRC, SBIS, SBIC, CPSE) that skips a 2-word instruction needs three clock cycles. If an interrupt occurs during the first or second clock cycle of this skip instruction, the return address will not be stored correctly on the stack. In this situation, the address of the second word in the 2-word instruction is stored. This means that on return from interrupt, the second word of the 2-word command will be decoded and executed as an instruction. The AT90S8515 has two 2-word instructions: LDS and STS.

Note 1: This can only occur if all of the following conditions are true:

- A skip instruction is followed by a 2-word instruction.
- The skip instruction is actually skipping the 2-word instruction.
- Interrupts are enabled, and at least one interrupt source can generate an interrupt.
- An interrupt arrives in the first or second cycle of the skip instruction.

Note 2: This will cause problems only if the address of the following LDS or STS command points to an address beyond 400 Hex.

Problem Fix/Workaround

For assembly program, avoid skipping a 2-word instruction if interrupts are enabled.

The following C-compilers handles this sequence correctly:

– IAR Compiler, version 1.40b or higher

– Image Craft compiler, all versions

Codevision Compiler, version 1.0.0.5 or higher

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